Circuit-design Perspective of Foundry Announced MRAM

Associate Prof. **Hao Cai**
National ASIC System Engineering Research Center
Southeast University

Outlines

1. Introduction
2. Emerging NVMs: State of the Art
3. Recent work on MRAM
4. Highlight of Energy-aware spintronics
5. Conclusion and Perspective

About me

- MsC, Lund Univ. 2009, PhD, TELECOM ParisTech, 2013
- Since 2018, Associate Prof., Southeast University, China,
  - Affiliation: National **ASIC** System Engineering Research **Center**
  - Emerging memory group: 1 Postdoc, 1 Phd, 12 MsC

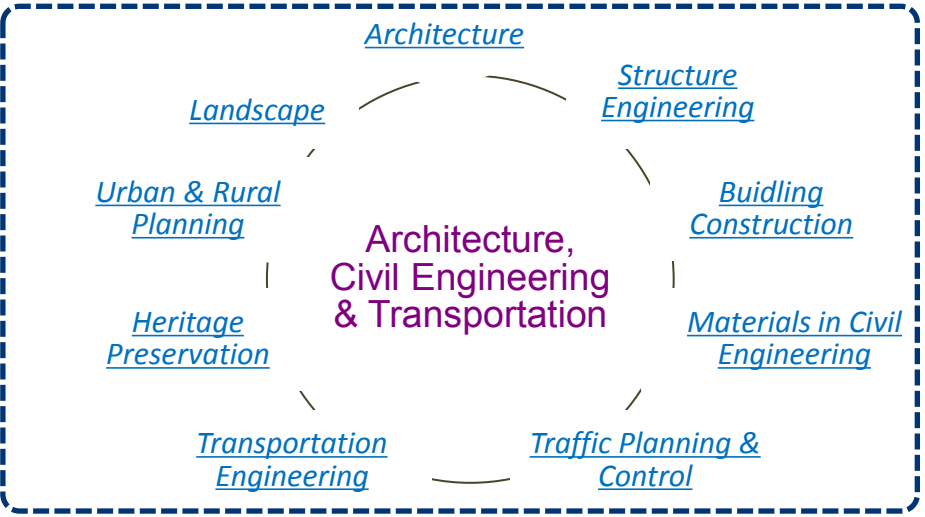
- Project Coordinator:
  - Speculative **MRAM** (NSFC, 2020),
  - **TFET**-VLSI (National Key Research and Development Program of China)
  - Partner: Energy-efficient DRAM (NSFC, 2018)

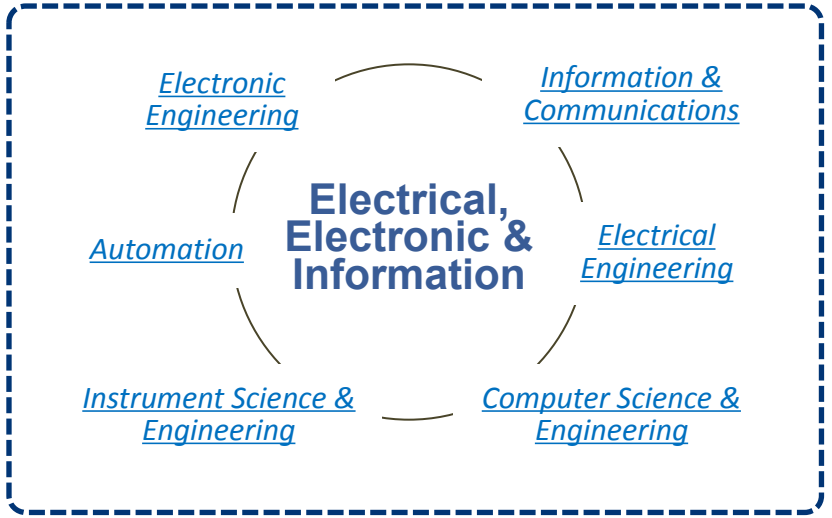
中华人民共和国科学技术部
Ministry of Science and Technology of the People´s Republic of China

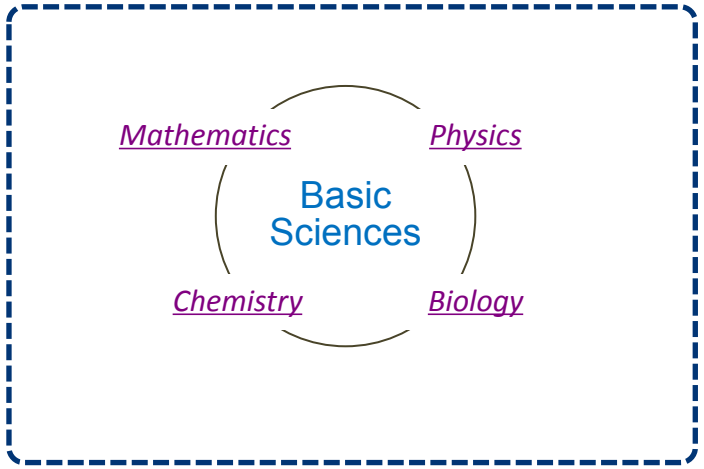
国家自然科学基金委员会
National Natural Science Foundation of China

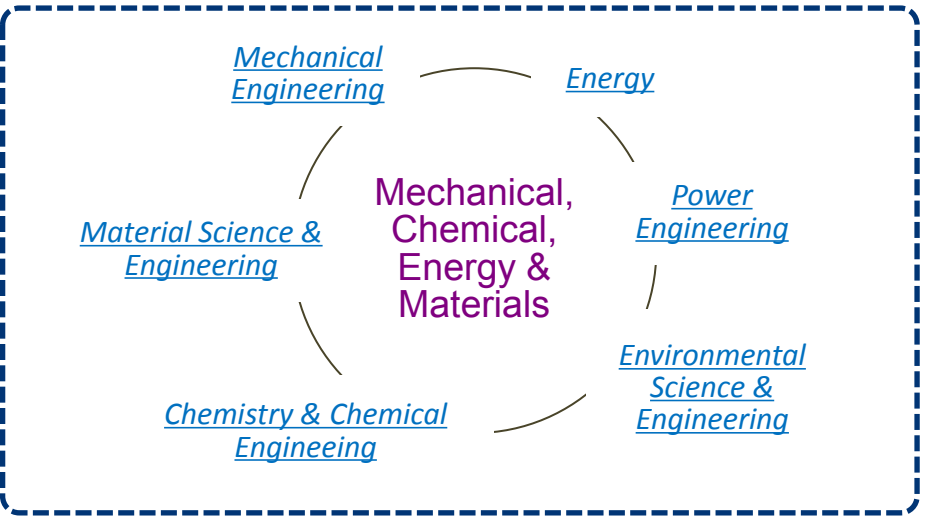
About Southeast University

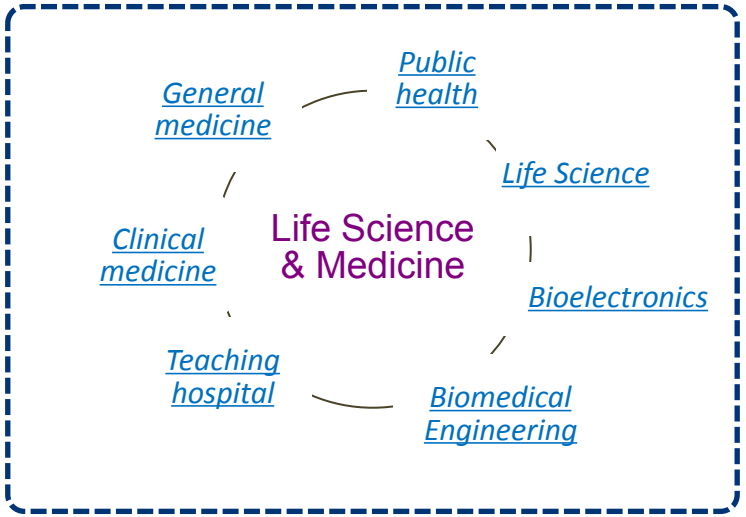
A research university, comprehensive with engineering as focus





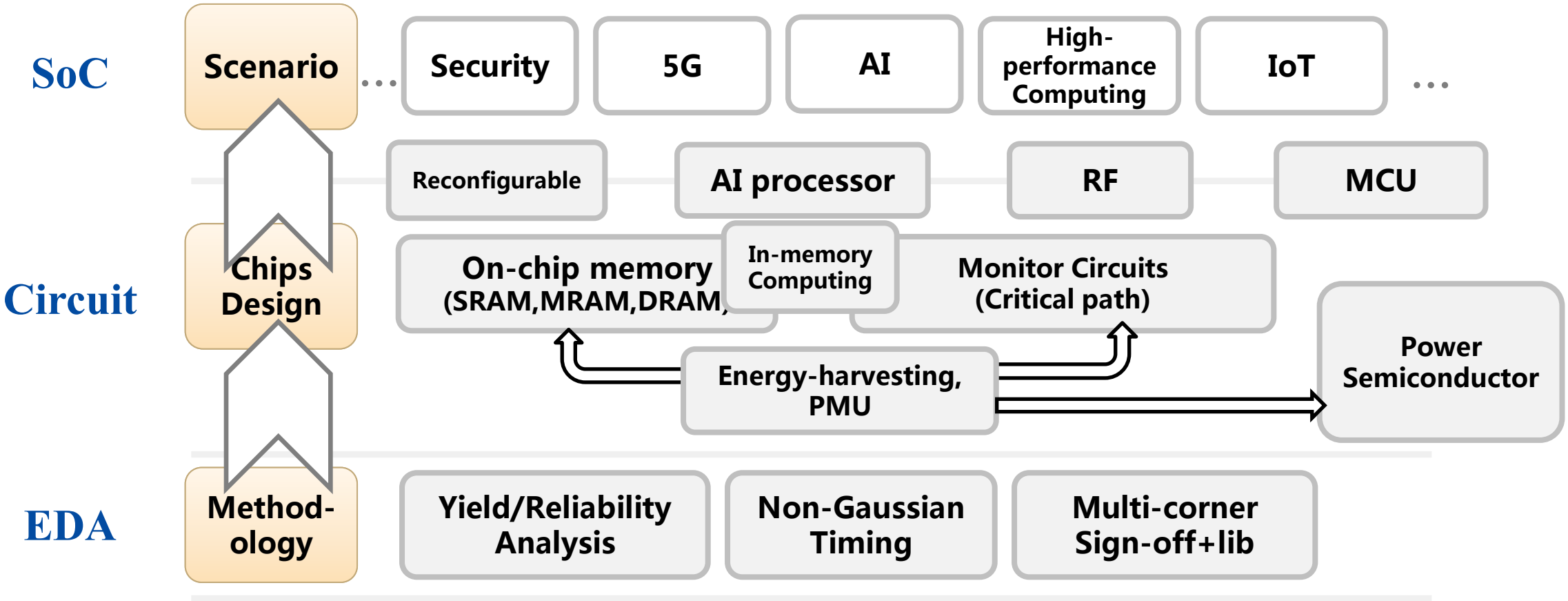






About ASIC Center (SEU)

National **ASIC** System Engineering Research **Center**



Discussion

- Research work during pandemic COVID-19
  - (1) on-line group meeting + deadline setup
  - (2) virtual conference participation (ISCA)
  - (3) proposal (funding)

- Why MRAM and low-power matter

- Importance of foundry participation
  - (1) integrated device manufacture (IDM, e.g., Everspin)
  - (2) TSMC + SMIC + Globalfoundry

Why it matters | Published: 27 April 2020

Coronavirus pushes education online

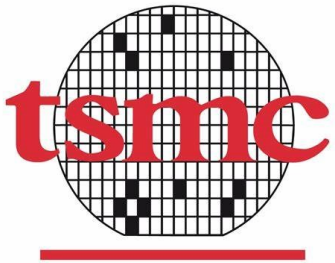
Litao Sun, Yongming Tang & Wei Zuo

Nature Materials **19**, 687(2020) | Cite this article

3137 Accesses | **9** Altmetric | Metrics

Litao Sun, Yongming Tang and Wei Zuo reflect on their experience of nationwide distance learning in China's universities during the COVID-19 outbreak.

The coronavirus disease 2019 (COVID-19) pandemic has shown scant respect for manmade borders and it took just three months to bring the world to a standstill, proving how intimately connected we are as earthlings. Following the outbreak of



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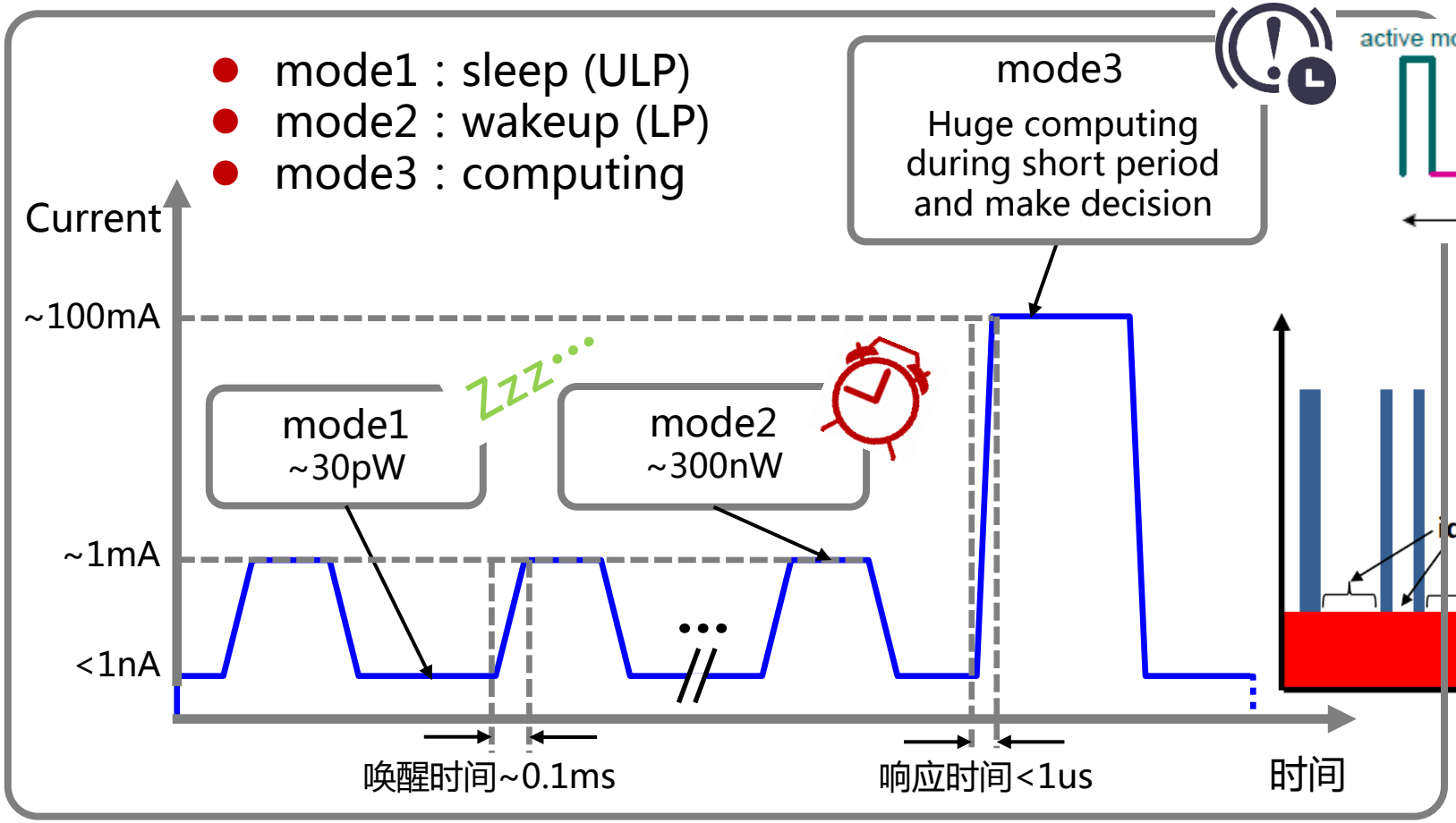
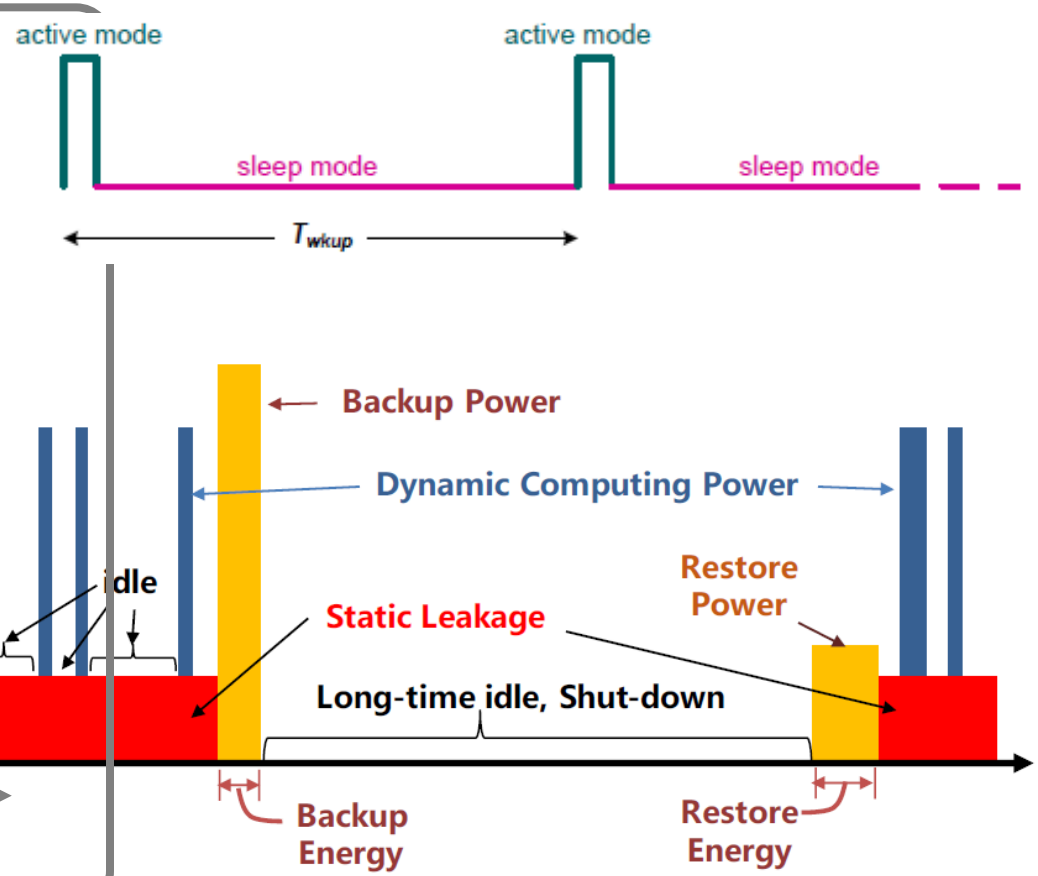
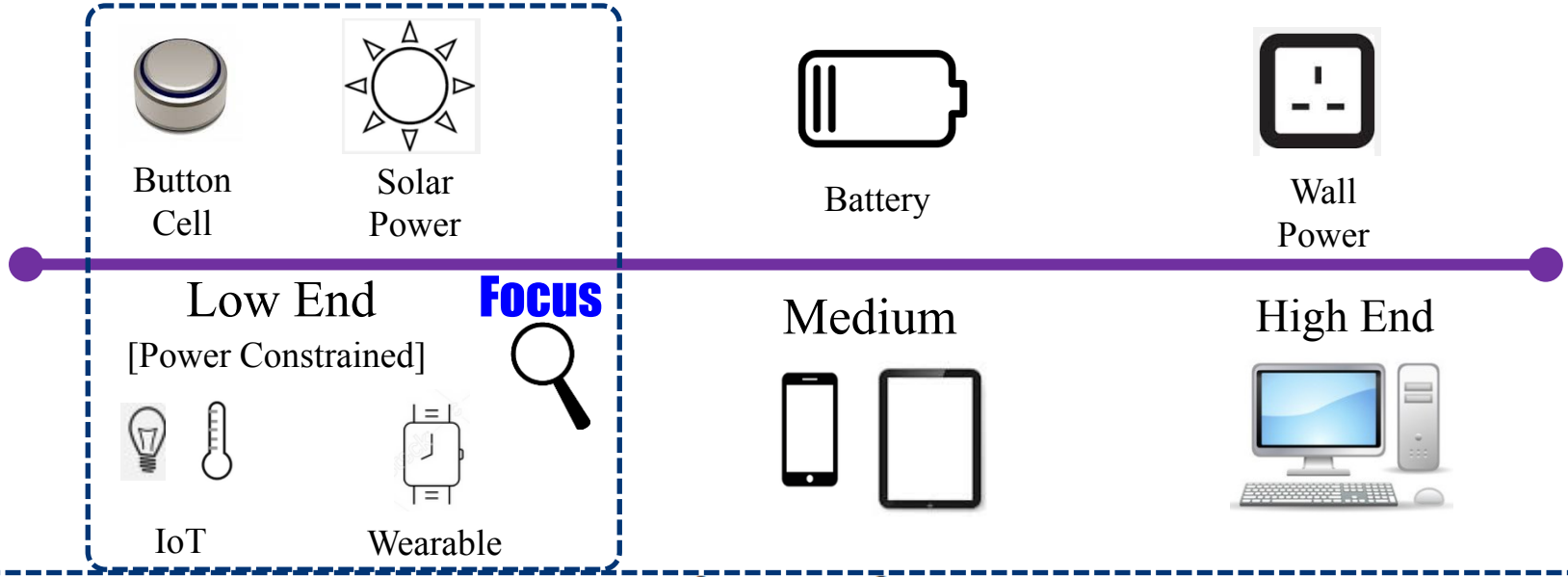
Importance of emerging memories (1)

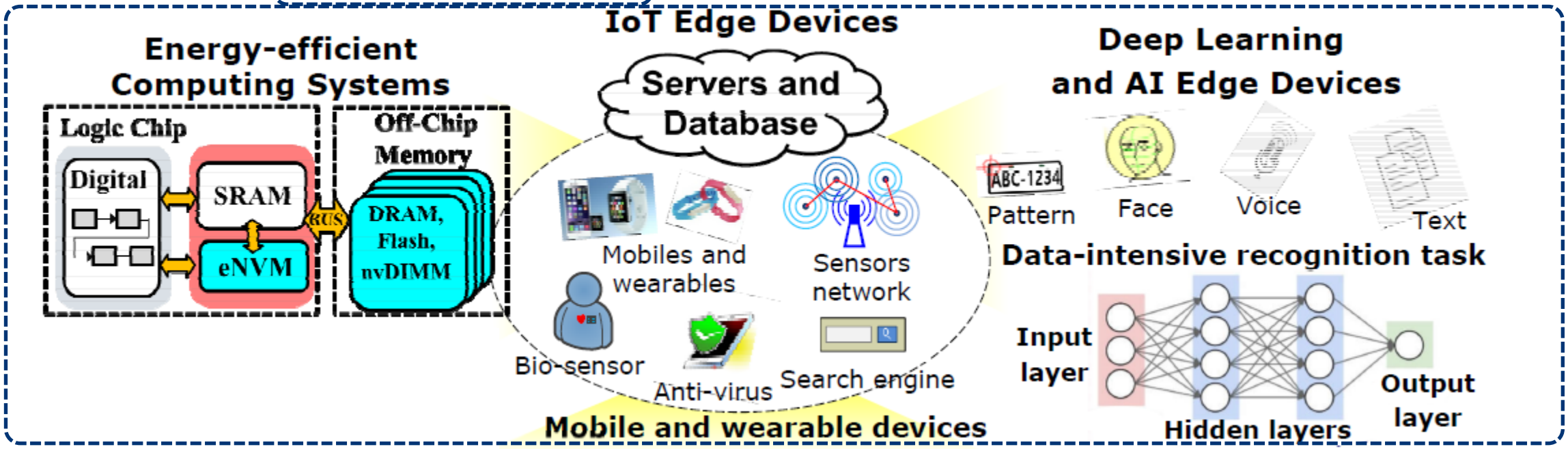
- Power management is the main concern in Moore's law/More Moore
- Emerging memories offer zero-leakage in the standby scenario





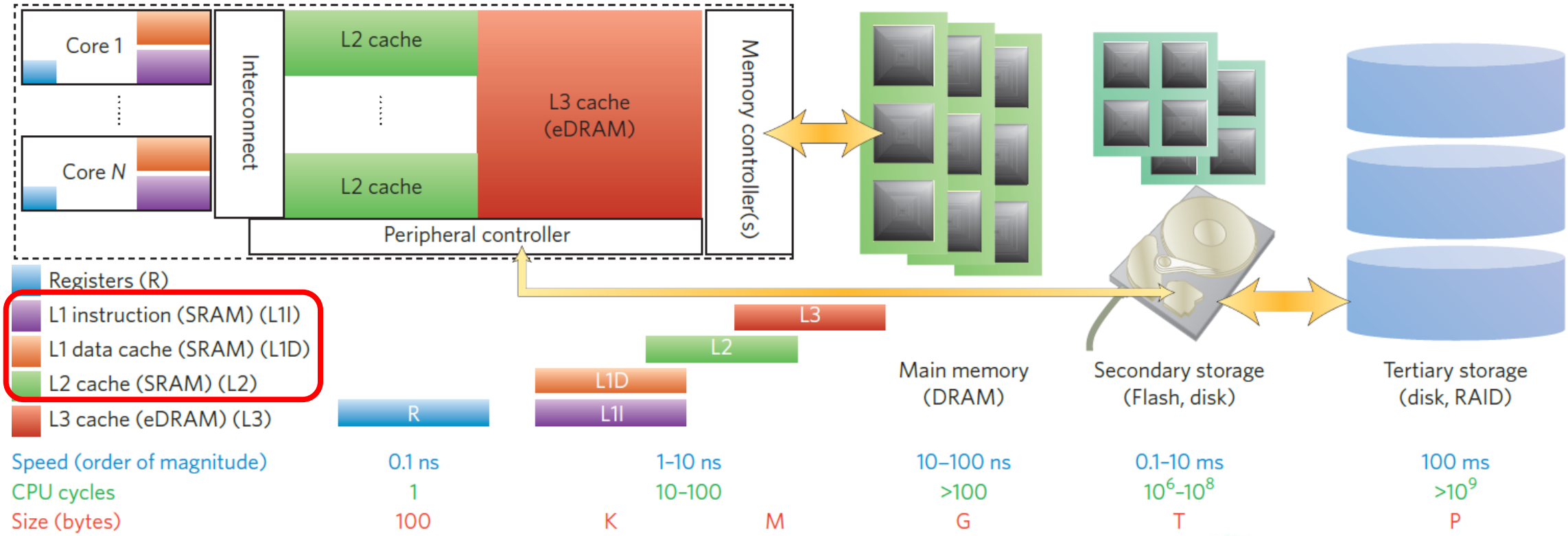
Importance of emerging memories (2)





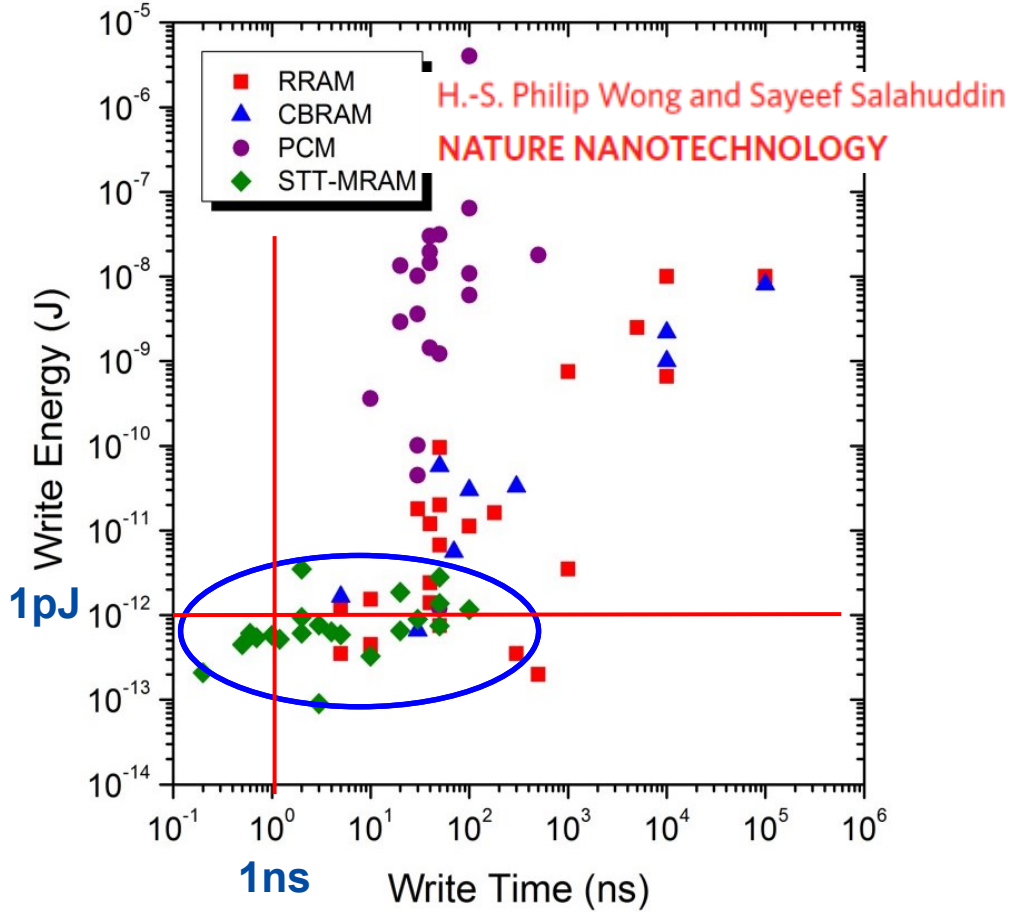
Energy-efficient on-chip memory

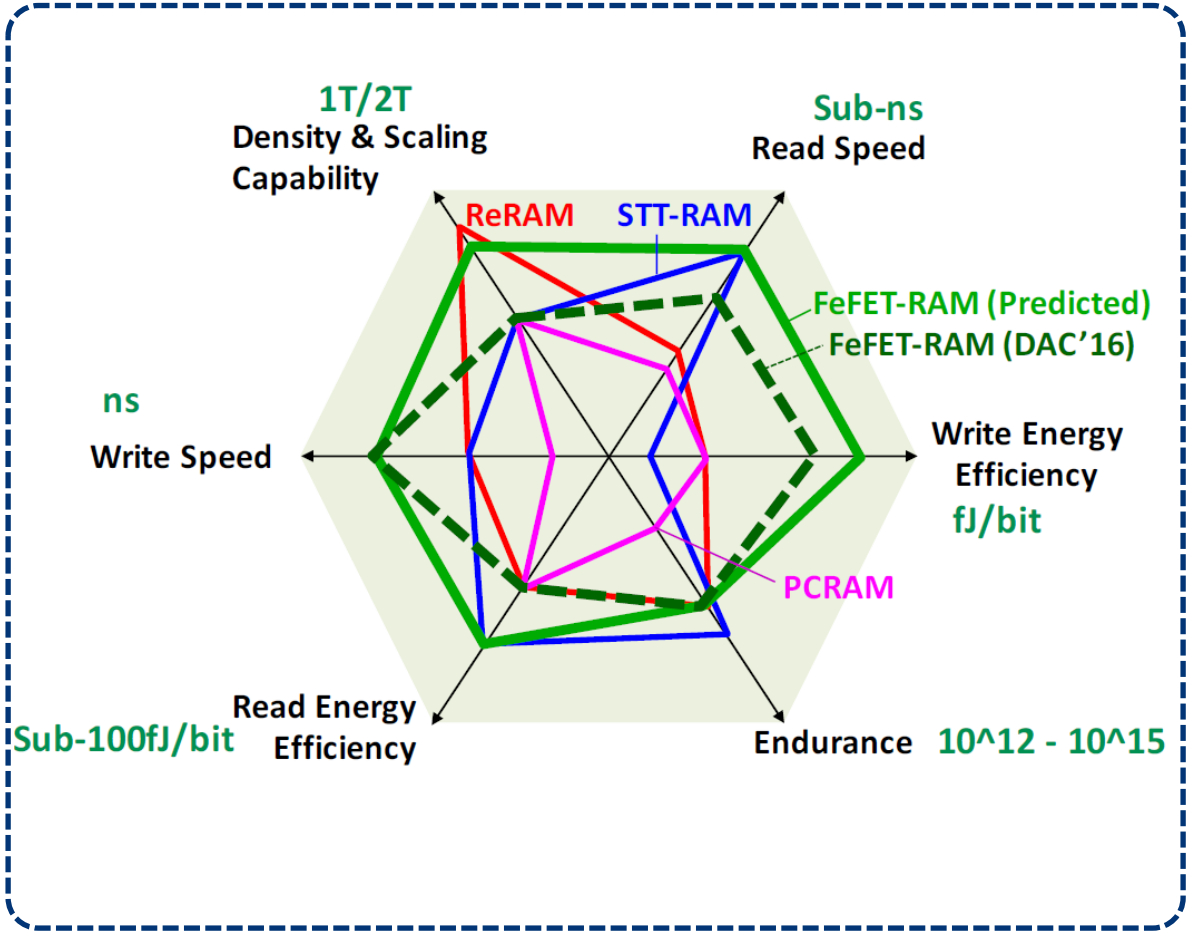
- Development of SRAM，innovation of std. unit/cache…
- Emerging memories replacement
- Non-von Neumann: Computing-in-memory



Typical emerging memories

- Main emerging non-volatile memories: RRAM, PCRAM, MRAM

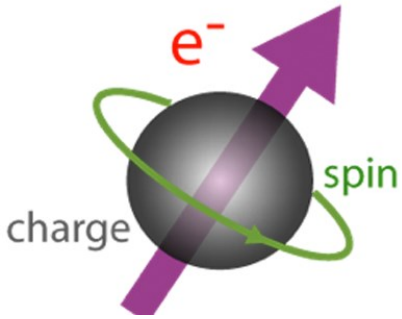




- Very-low write energy~1pJ
- Bottleneck: cost and efficiency

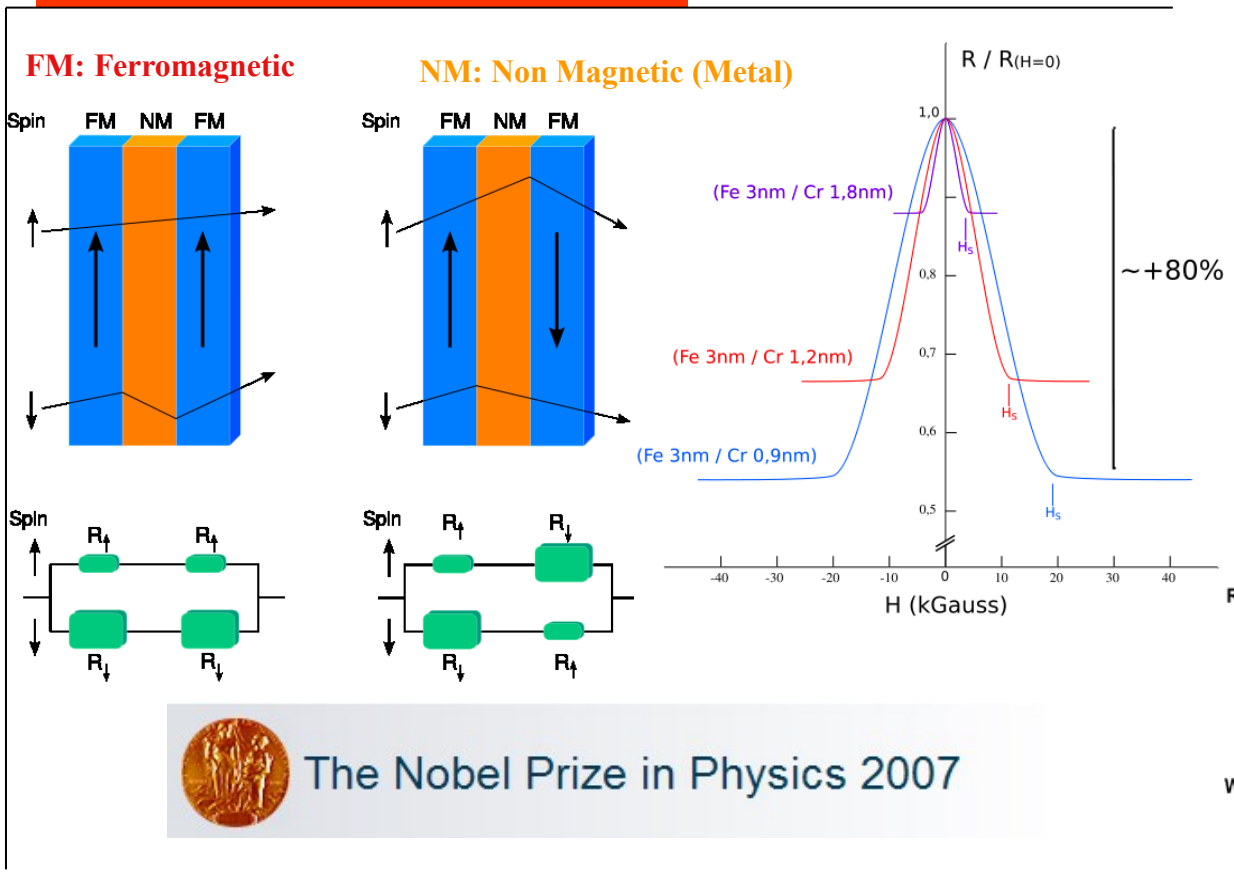
Spintronic device

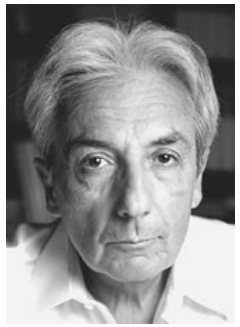
"Electron does not have only a charge, but also a spin" Is it possible to construct a practical electronic device that operates on the spin of the electron, in addition to its charge?



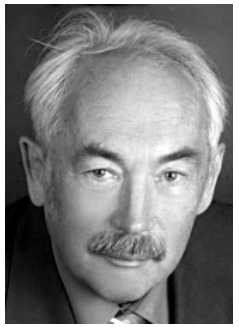
Giant MagnetoResistance (GMR)

A.Fert et al., PRL, 1988





Albert Fert

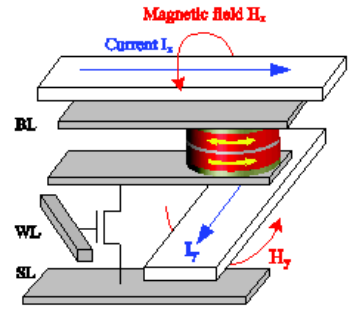


Peter Grünberg

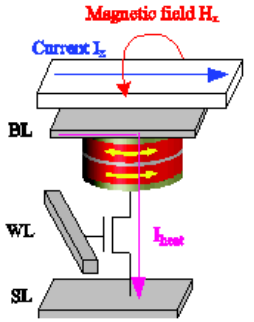
Forschungszentrum Jülich
in der Helmholtz-Gemeinschaft

The Nobel Prize in Physics 2007

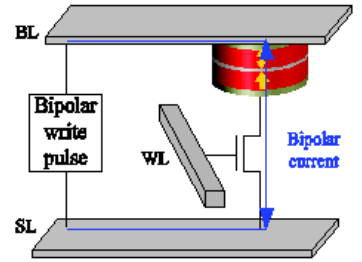
Claude Chappert, Albert Fert, *Nature Materials,* 2007



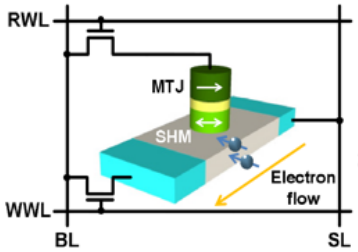
Toggle MRAM



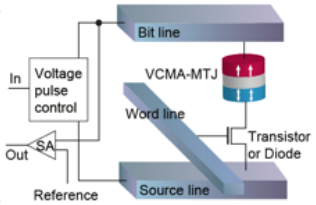
TAS-MRAM



STT-MRAM



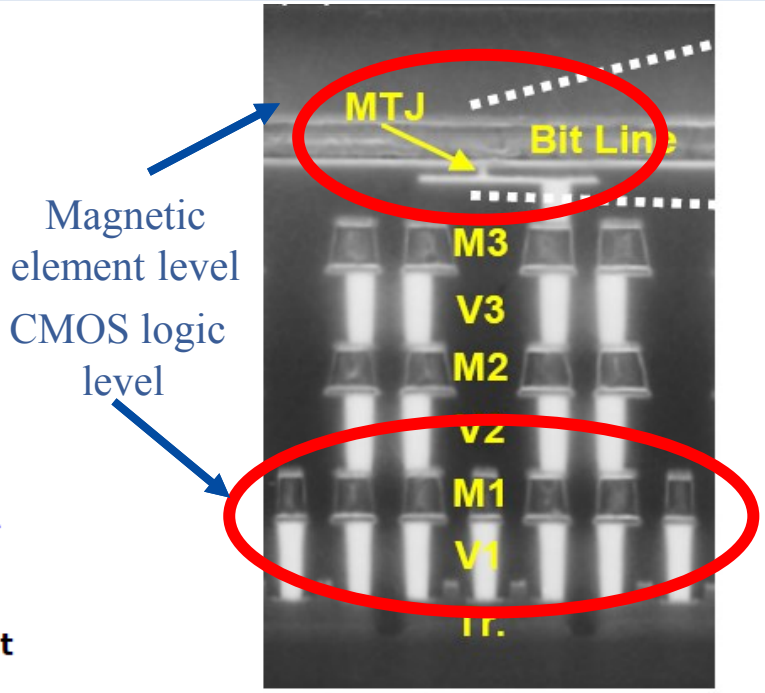
SOT-MRAM



VCMA-MRAM

Fabrication last ten-years for MRAM

- Perpendicular MTJ with STT switching is with industry recognition, located at the high metal layer
- Smaller bit-cell and larger capacity



STT-MRAM Development Status

2009
- 12ns 32Mb MRAM chip @ISSCC — NEC

2010
- 64Mb STT-MRAM chip @ISSCC — TOSHIBA

2011
- 45nm 1Mb STT-MRAM @VLSI — QUALCOMM
- Joint Develop Contract — SK hynix, TOSHIBA
- Samsung buys Grandis — SAMSUNG
- Micron Collaborates With A*Star DSI — Micron
- 17nm PMTJ evaluation — SAMSUNG

2012
- Everspin 64Mb DDR3 product –First Commercial STT-MRAM — EVERSPIN TECHNOLOGIES

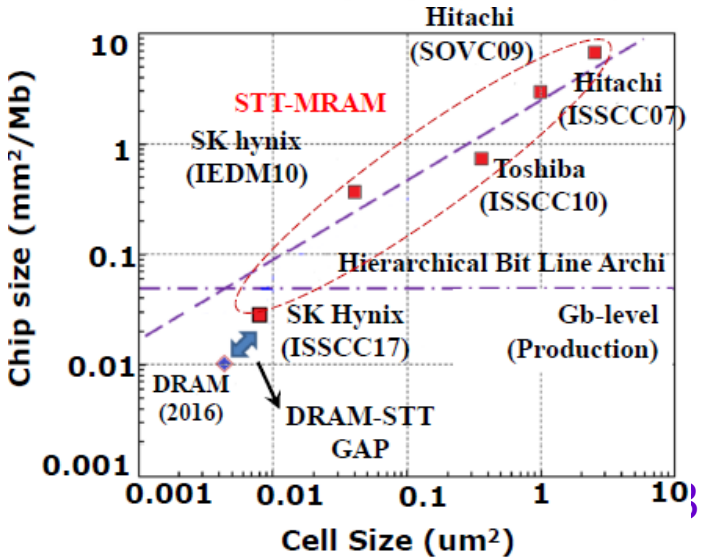
2013
- 40nm 1Mb, 1.1/2.5V, 10ns @ISSCC — tsmc
- 8Mb, 1.1V,TDSA, 3ns-read @ISSCC — Infineon

2015
- 8Mb, 1.5V, TMR=200%, 9.1ns-read @ISSCC — SAMSUNG
- 65nm 1Mb, 1.2V, 3.3ns STT-MRAM @ISSCC — TOSHIBA

2016
- Low-power 4Mb STT-MRAM Cache @ISSCC — TOSHIBA

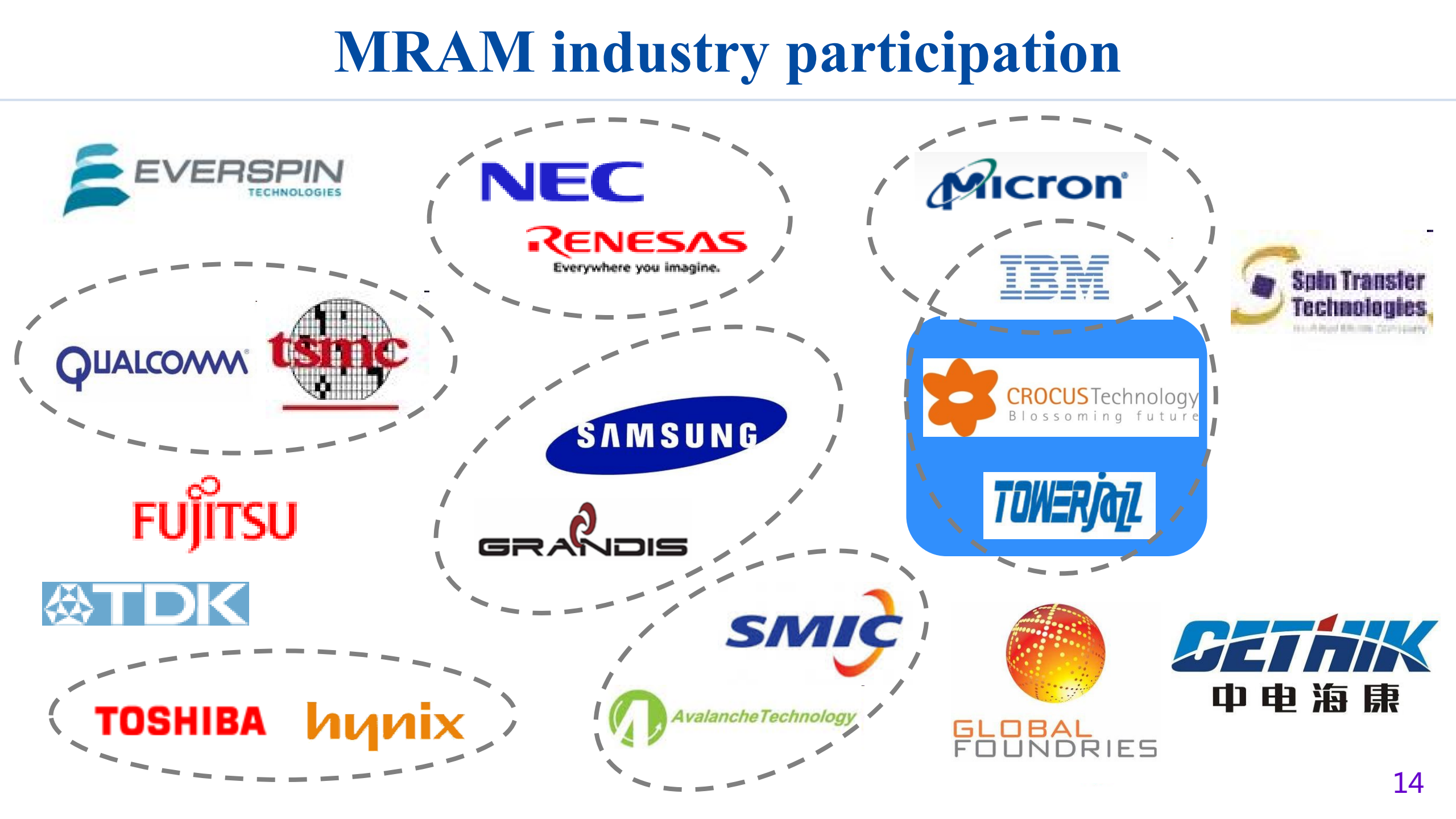
2017
- 4Gb LPDDR2 @ISSCC — SK hynix, TOSHIBA

2018
- 28nm 1Mb 1T1MTJ 2.8ns-read @ISSCC — University of Michigan, tsmc
- 28nm 32kb 2T2MTJ 1.3ns-read @ISSCC



Copyright: Prof. M. F. Chang, ISSCC18 Tutorial

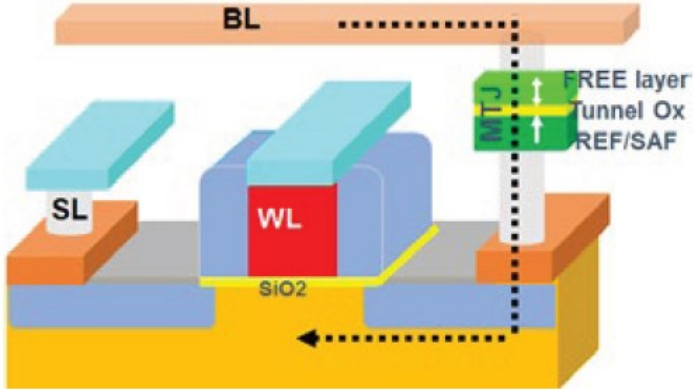
MRAM industry participation



Foundry announced MRAM info

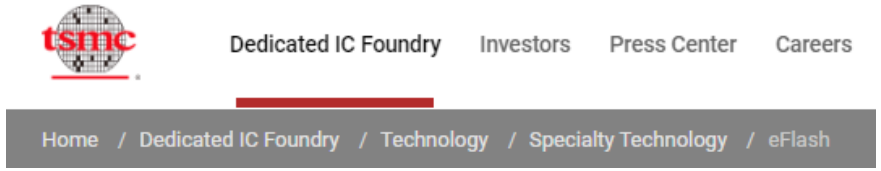
Key Features

- Versatile embedded memory in FD-SOI
- Energy efficient
- Fast write enables OTA updates
- Fast system wake-up
- No static leakage through eMRAM bitcell
- Fully integrated embedded memory solution with 22FDX® technology extensions
- Ideal for IoT, storage and compute applications



eMRAM Bit Cell

Copyright Globalfoundaries



Meanwhile, TSMC started volume production of 40nm Embedded Flash technology for automotive in 2018, and is now developing the 28nm Embedded Flash. This technical qualification is expected in 2019 for automobile electronics and micro controller units (MCU). At the mean time, TSMC is also developing Embedded MRAM, and Embedded RRAM in parallel to fulfill customers' need of continuous performance improvement and power-consumption reduction. 40nm ULP embedded resistive random access memory (RRAM) technology, which began risk production at the end of 2017, completed consumer grade qualification test for 10,000 cycles of endurance in 2018. This technology is fully CMOS (Complementary Metal Oxide Semiconductor) logic compatible for PDK and IP re-use for applications including wireless MCU, IoT and wearable devices. 22nm ULL magnetic random access memory (MRAM) technology progressed well, demonstrated reflow capability and passed JEDEC 168 hours high-temperature operating life (HTOL) reliability validation at the end of 2018. Through IP customization, MRAMs can serve various applications, such as artificial intelligence and eFlash replacement for MCU.

TSMC: https://www.tsmc.com/english/dedicatedFoundry/technology/eflash.htm

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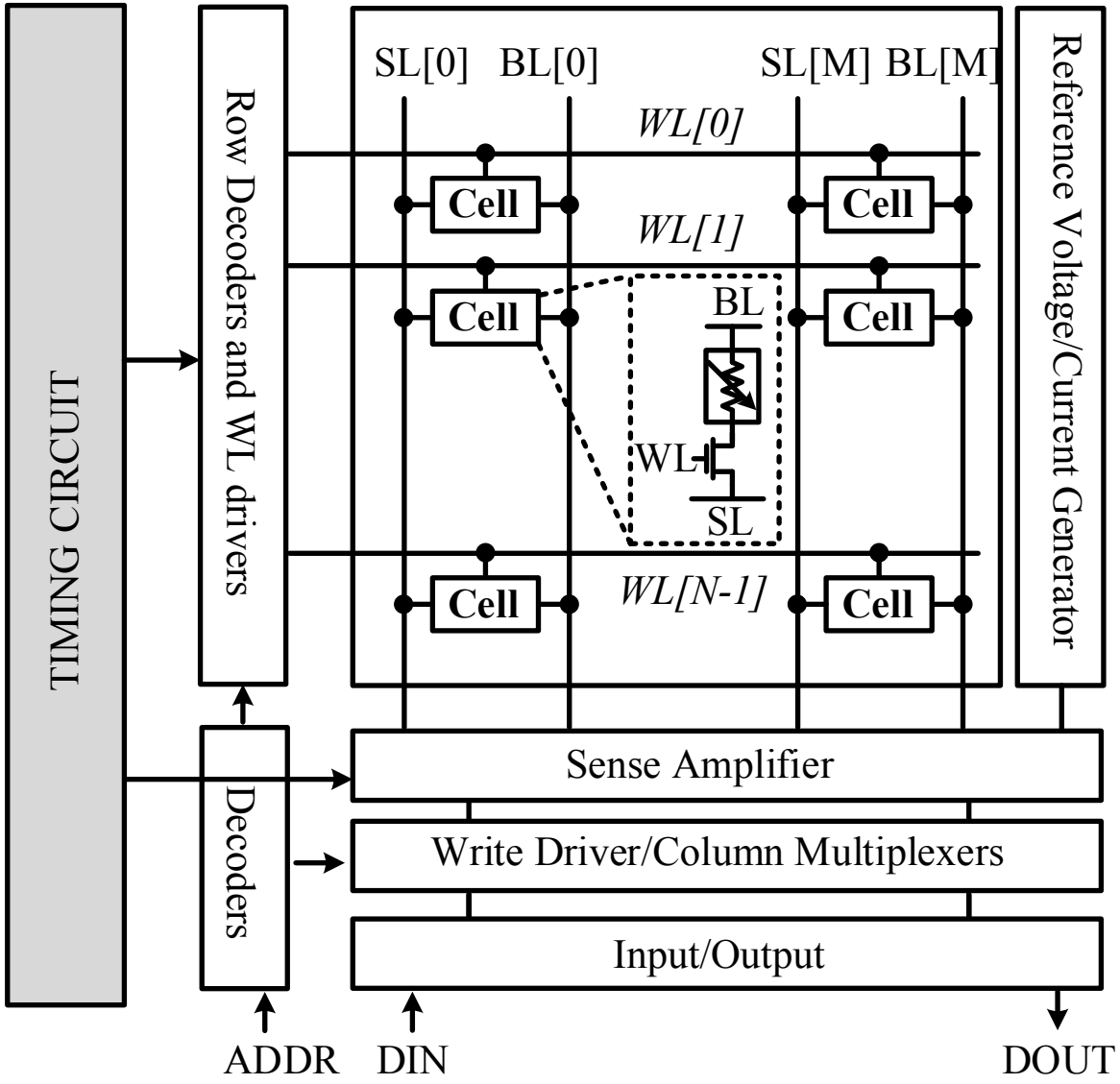
Recent work of MRAM (1)



- MRAM macro building blocks optimization

- Row/Column decoder/driver
- Timing Circuit
- Sensing amplifier
- Reference/current source
- Input/output

- Analog design flow
- Hybrid simulation using Verilog-A MTJ model and SPICE netlist

Recent work of MRAM (2)

Y. Zhou, H. Cai et al, IEEE TCAS-1 2020

- Self-timed voltage-mode sensing scheme:
  - Self-timed **sensing scheme** dynamically tracking the V_{BL} swing

Y. Zhou, H. Cai et al, IEEE TCAS-2 2020

- MTJ-based loop replica BL timing circuit
  - MTJ-based Loop Replica BL as **device-circuit interaction** for PVT-robust sensing

Y. Zhou, H. Cai et al Microelec. Rely. 2020

- Aging/Temperature monitored built-in self test (BIST)
  - Self-activated BIST by aging/temperature **monitoring scheme**

① New memory access schemes, ② device-circuit interaction

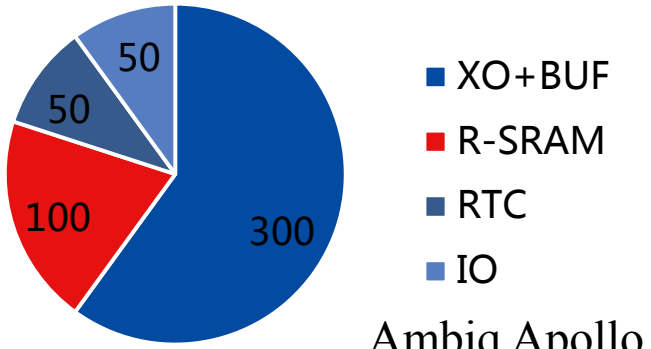
Recent work of MRAM (3)

Macros	Flash-like	SRAM-like
Bit-cell	1T-1MTJ	2T-2MTJ
Access time (R/W)	25ns/200ns	12.5ns/40ns
Retention	> 10 years	> 10 years
Endurance	**> 1M cycles**	> 100 M cycles
Energy	1 pJ/bit	1 pJ/bit

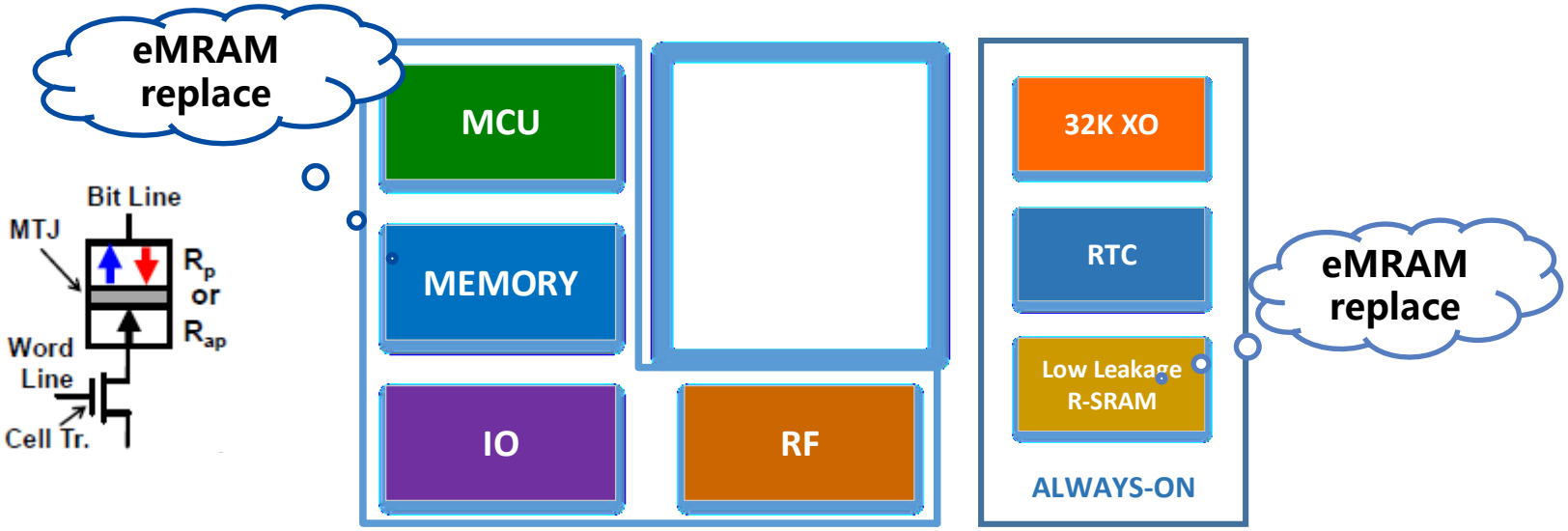
Source: Globalfoundaries

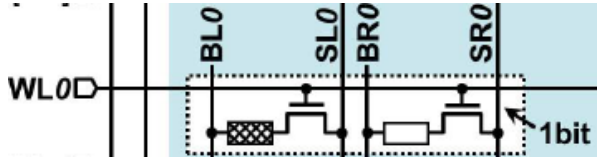
Typical sleep current

(nA)



Ambiq Apollo
STM32L4xx
ADCuM3027

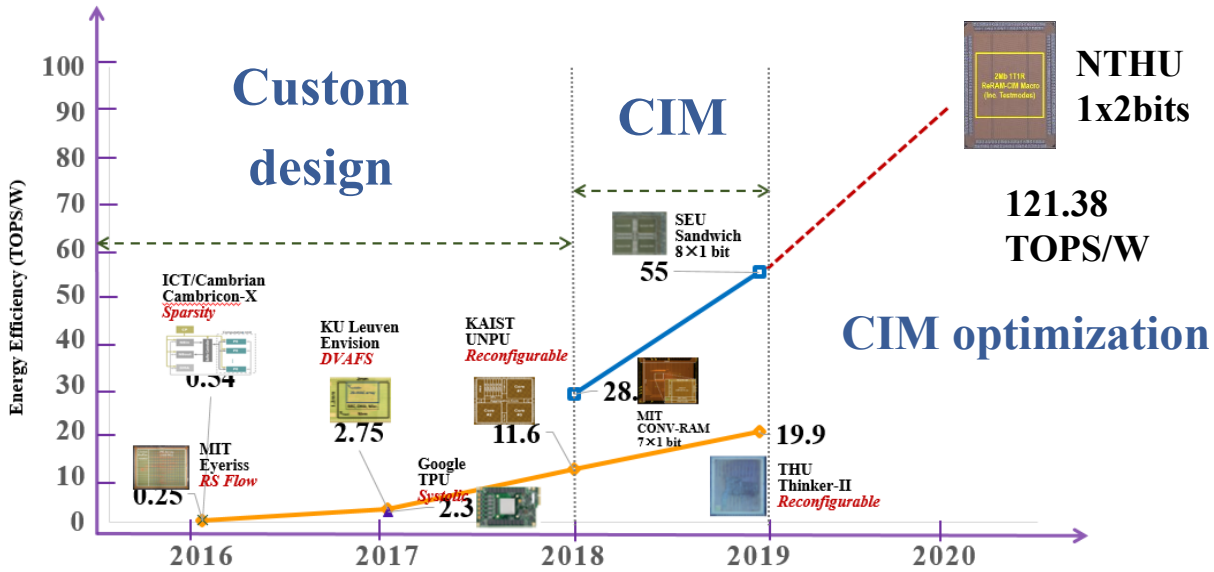




2T-2MTJ bit-cell

Perspective 1: computing-in-memory

- Energy efficiency is the critical specification, great higher than Moore
- 50% energy in DRAM/SRAM
- CIM is with great challenge for custom interaction design



Recent CIM Silicon Development Status

SRAM-CIM

6T-SRAM Classifier @VLSI16, (Princeton)

4+2T SRAM @ VLSI17 (Princeton)

BRein Memory @ VLSI17 (Hokkaido)

10T CSRAM BWN @ ISSCC18 (MIT)

Classifier SVM @ ISSCC18 (UIUC)

DSC6T SRAM BNN @ ISSCC18 (NTHU)

XNOR-SRAM @ VLSI18 (Columbia)

4b T8T SRAM CNN @ ISSCC19 (NTHU)

AI-Accelerator+T-SRAM @ISSCC19, (THU+NTHU)

Sandwich RAM BWN @ISSCC19, (Southeast Univ.)

Compute SRAM + Accelerator @ISSCC19, (Michigan)

Time-based SRAM+ Accelerator @ISSCC19, (Minnesota)

SRAM+CNN video processor @ISSCC20(THU)

SRAM+CNN sparsity @ISSCC20 (THU+NTNU)

2016 | 2017 | 2018 | 2019 | 2020

ReRAM-CIM

32*32 RRAM FCN Binary/Ternary, 3b out @VLSI17 (THU&NTHU)

16Mb RRAM Logic @IEDM17 (NTHU)

1Mb RRAM CNN Binary/Ternary, 3b out @ISSCC18 (NTHU)

224b SLC RRAM @ISSCC18 (Stanford)

2Mb RRAM FCN MLC cell+binary out

1Mb RRAM 2bIN/3bW CIM @ISSCC19

@ISSCC20 ReRAM+Neurosynaptic (Stanford)

ReRAM+MAC @ISSCC20 (THU+NTNU)

ISSCC 2020 first MRAM CIM

A 22nm 1Mb 1024b-Read and Near-Memory-Computing Dual-Mode STT-MRAM Macro with 42.6GB/s Read Bandwidth for Security-Aware Mobile Devices

Tung-Cheng Chang, Yen-Cheng Chiu, Chun-Ying Lee, Je-Min Hung, Kuang-Tang Chang, Cheng-Xin Xue, Ssu-Yen Wu, Hui-Yao Kao, Peng Chen, Hsiao-Yu Huang, Shih-Hsih Teng, Meng-Fan Chang

National Tsing Hua University, Hsinchu, Taiwan

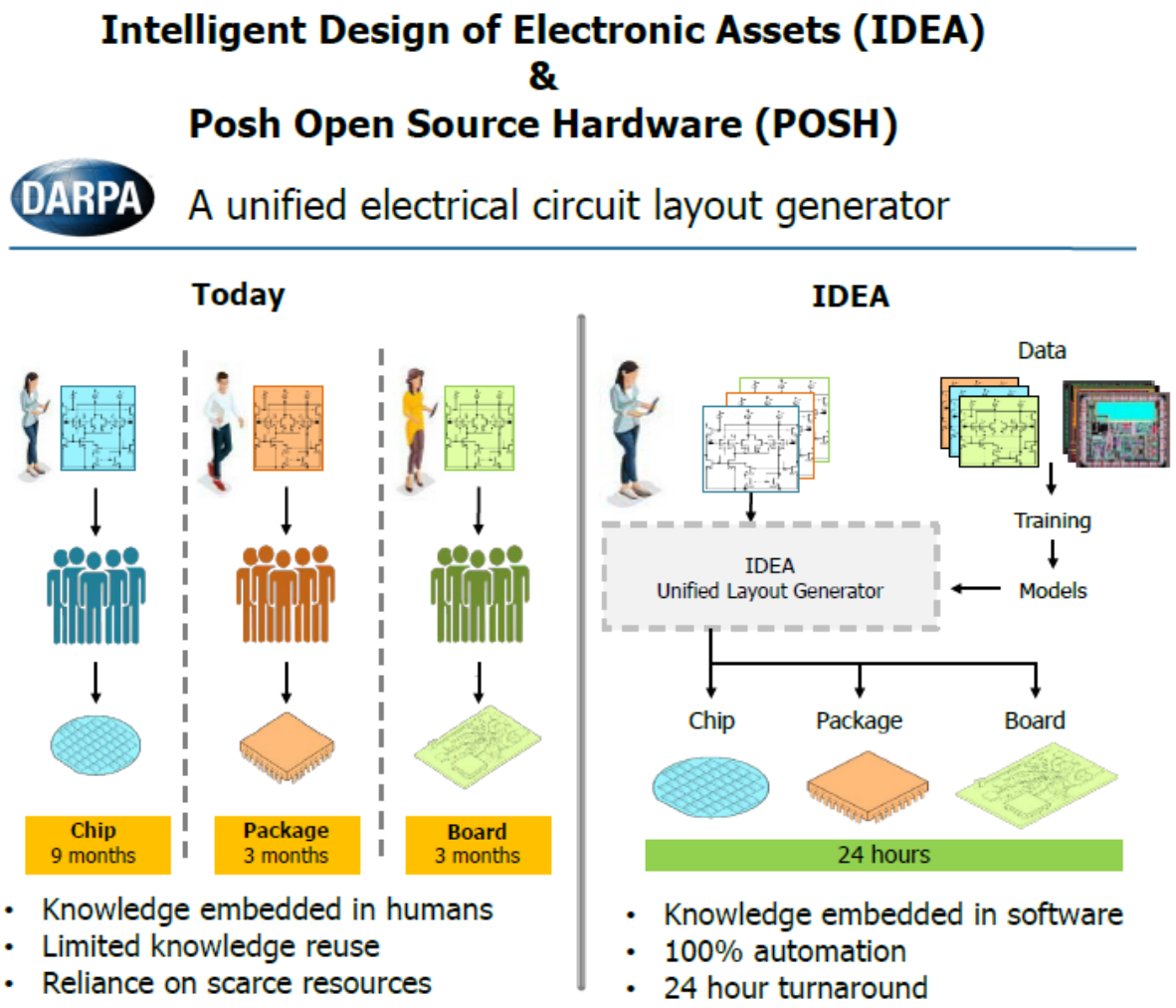
TSMC, Hsinchu, Taiwan

國立清華大學 NATIONAL TSING HUA UNIVERSITY

Prof. M. F. Chang, ISSCC20

Perspective 2: EDA-compatible

- Emerging memories/new device, EDA-compatible



IDEA aims to create a "no human in the loop" 24 hour turnaround layout generator for System-On-Chips, System-In-Packages, and Printed Circuit Boards.

New procedures for physical design and verification will lower the design barrier, enabling rapid specialization

Design

Intelligent Design of Electronic Assets (IDEA)

- No human in the loop" 24-hour layout generation for mixed signal integrated circuits, systems-in-package, and printed circuit boards.Machine generated layout of electrical circuits and systems

Verification

Posh Open Source Hardware (POSH)

- An open source System on Chip (SoC) design and verification eco-system that enables cost effective design of ultra-complex SoCs.

Source: DARPA 2017

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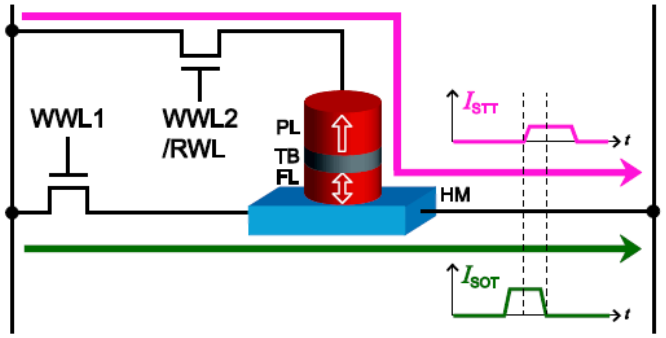
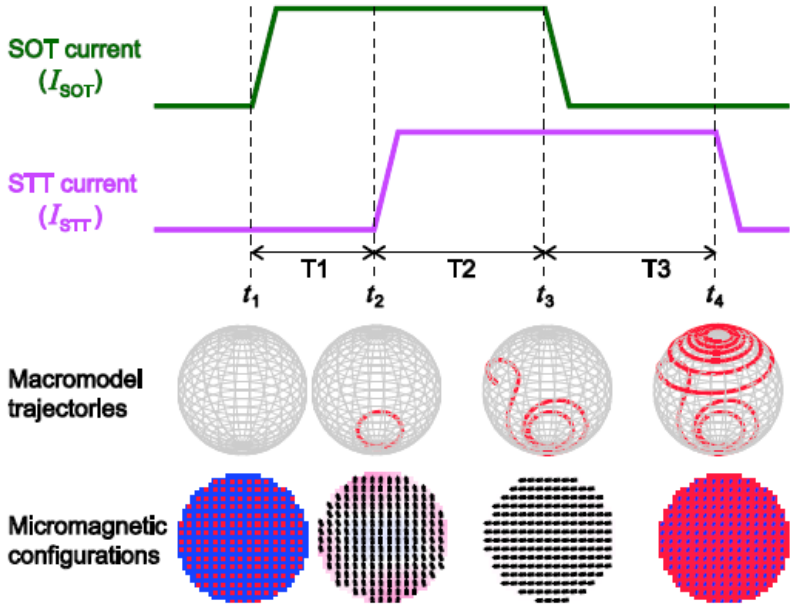
Energy-aware spintronics – device level

Interplay switching of MRAM bit-cell

SOT+STT

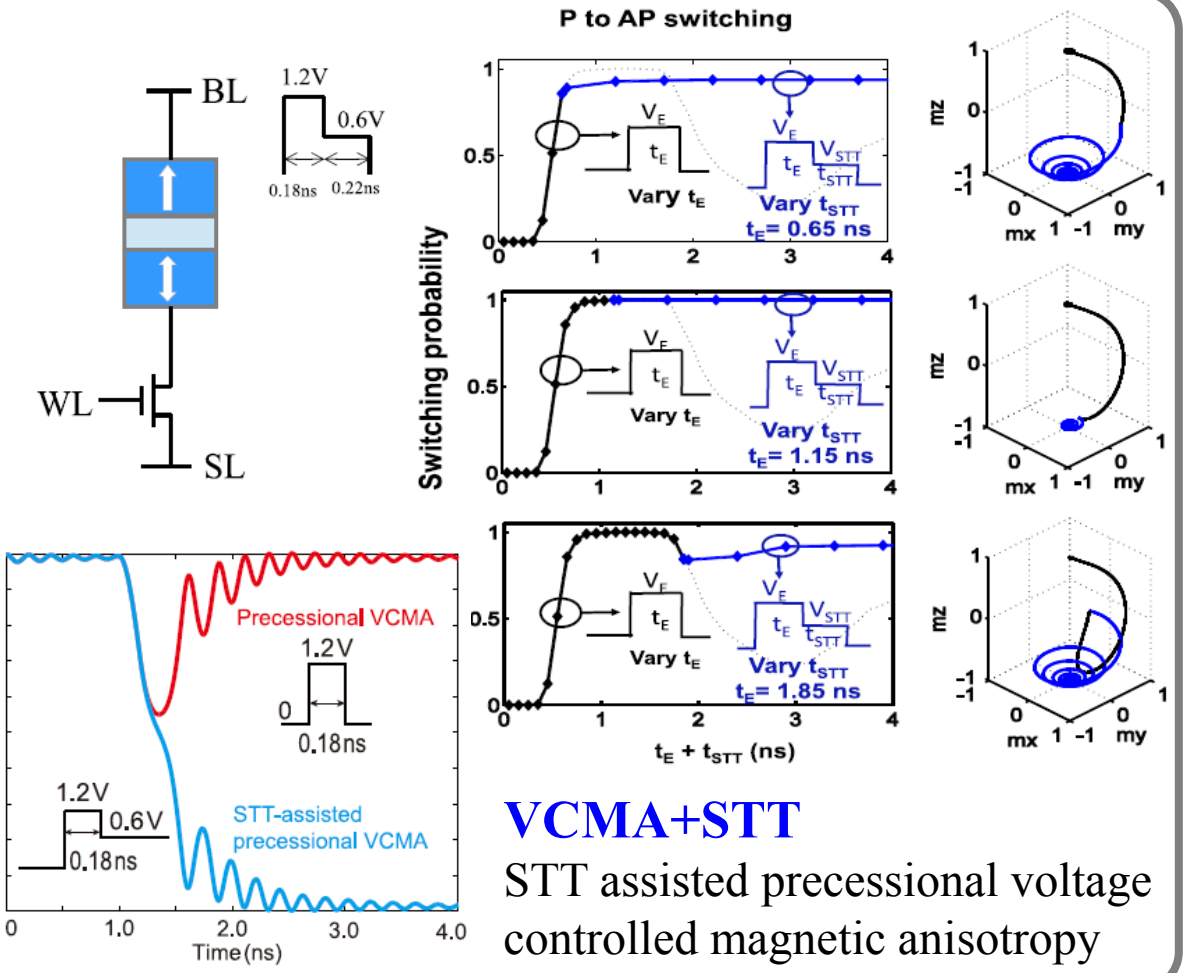
I_{sot} and I_{stt} are sequentially applied to the device in the toggle-like manner.





t_1: only SOT
t_2: STT&SOT interplay effect
t_3: SOT remove
t_4: relax

Zhao et al, Nat Elec 19
Wang et al, EDL 19
Roy et al, TED 17



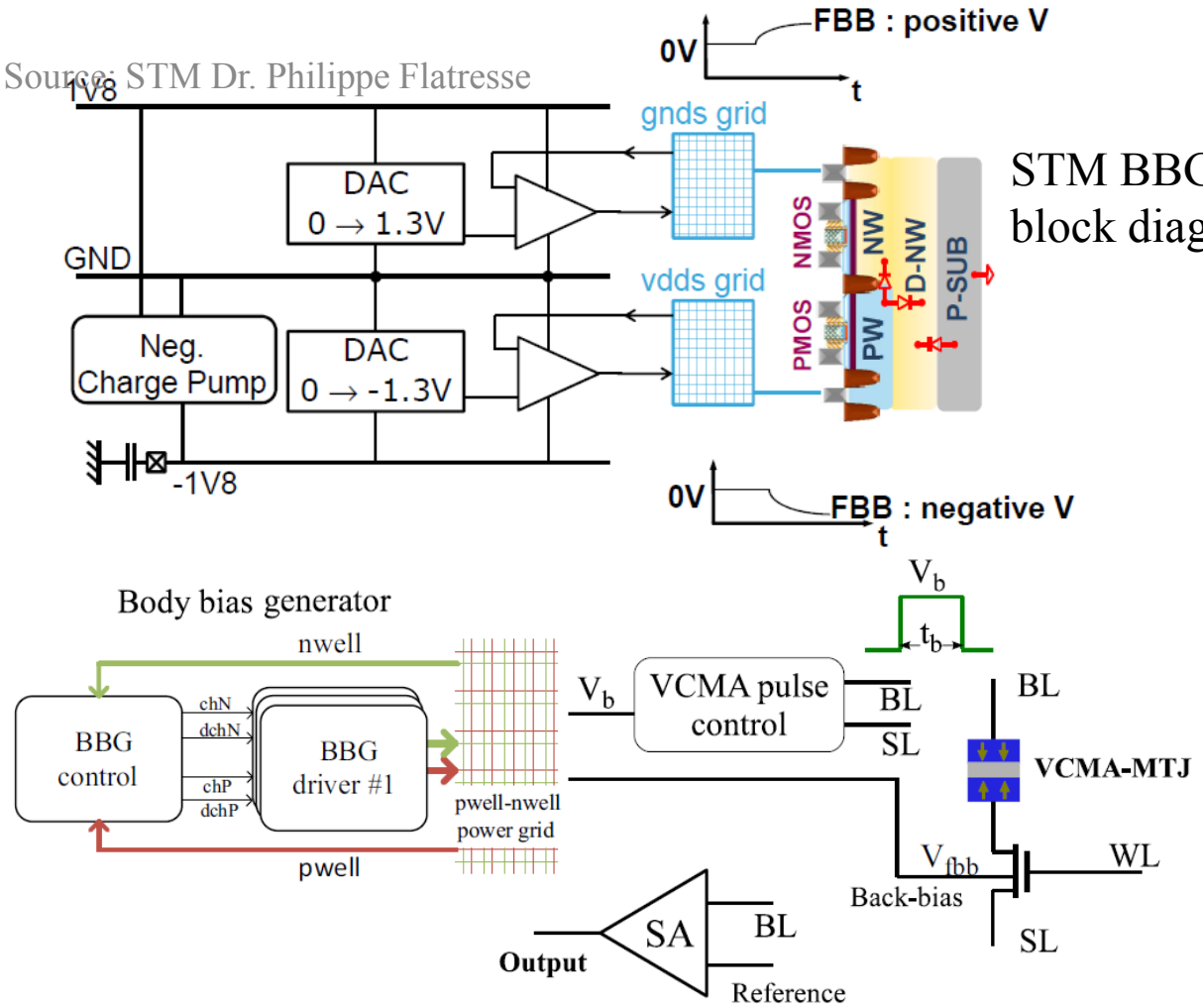
VCMA+STT

STT assisted precessional voltage controlled magnetic anisotropy

Energy-aware spintronics – circuit level

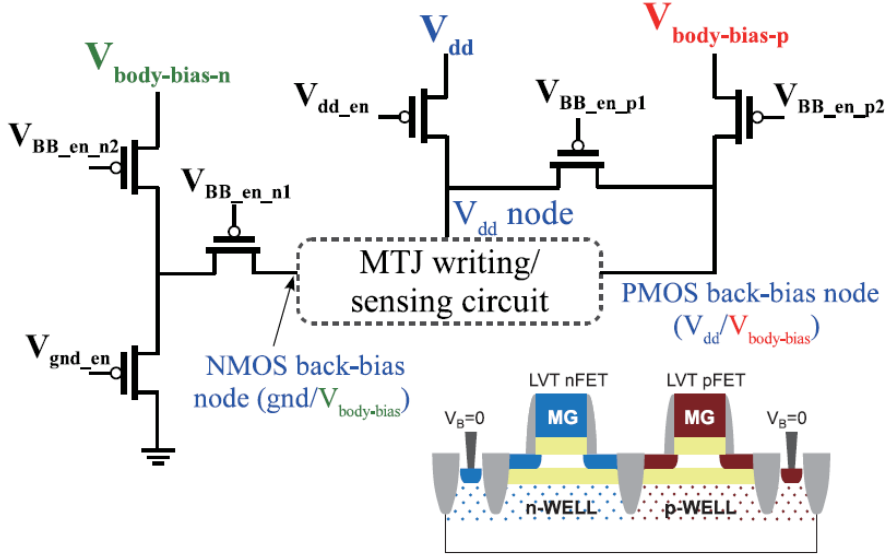
MRAM-on-FDSOI design strategy

Source: STM Dr. Philippe Flatresse



STM BBG IP block diagram

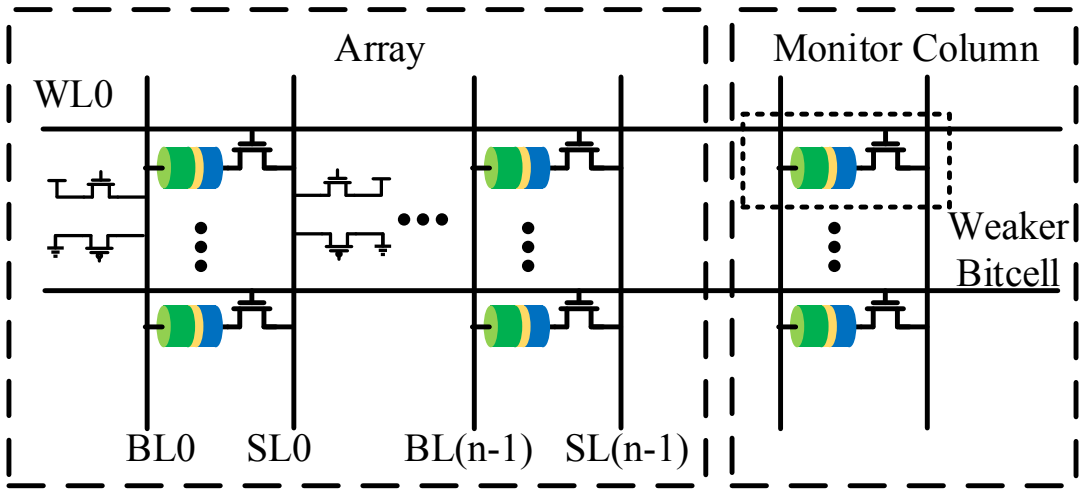
- Body-bias generator method
- Flip-well method



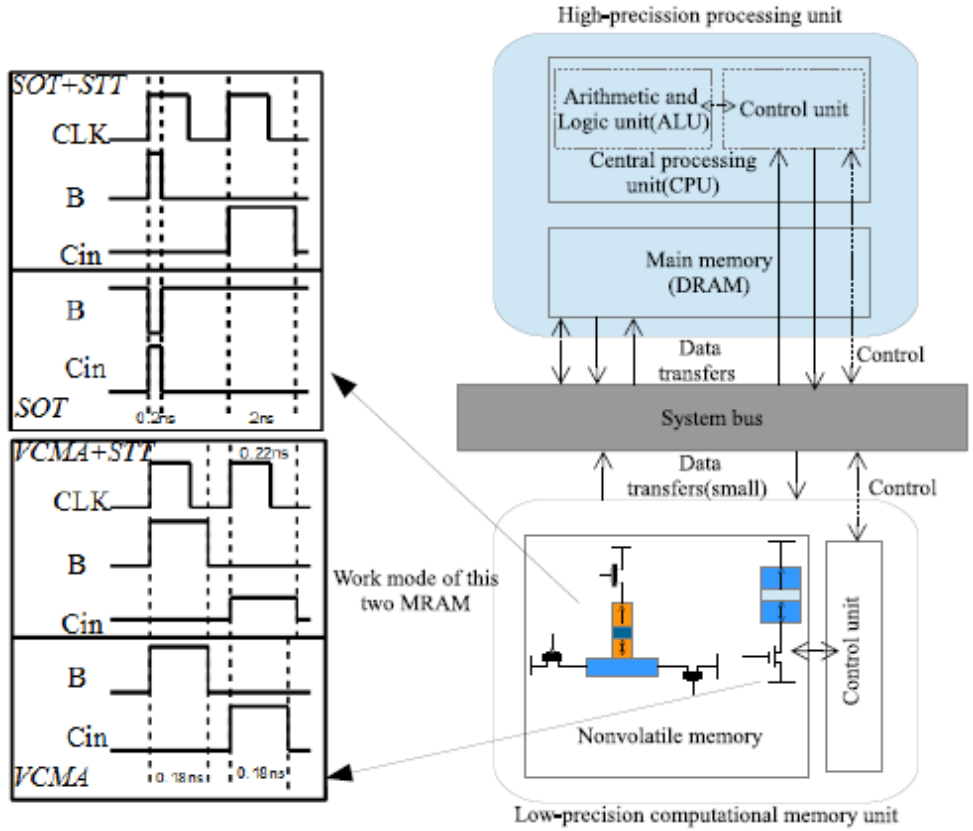
The programmable body-bias generator (BBG) with a step-size of 100 mV is used to generate VCMA pulse and forward body-bias voltage

Energy-aware spintronics – system level

Speculative strategy, approximate MRAM



- Conventional common writing timing waits the weak bit-cell as Unnecessary power consumption
- Proposed Speculative scheme uses weak bit-cell to monitor the writing operation as PVT tracking writing timing circuit



Mixed precision MRAM

Outlines

1. Introduction
2. Emerging NVMs: State of the Art
3. Recent work on MRAM
4. Highlight of Energy-aware Circuits
5. Conclusion and Perspective

Conclusions and perspective

- COVID-19 is an interlude event in the research work.
- MRAM could be the next-generation working memory, to replace eFlash and L3 cache. Now the major stumbling block is the ‘cost’.
- Multi-level interaction design is an important methodology for MRAM
- Foundry (industry) can boost research.