Sensing interfacing in the edge: small, sound, smart !

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KATHOLIEKE UNIVERSITEIT LEUVEN

Abstract & biography

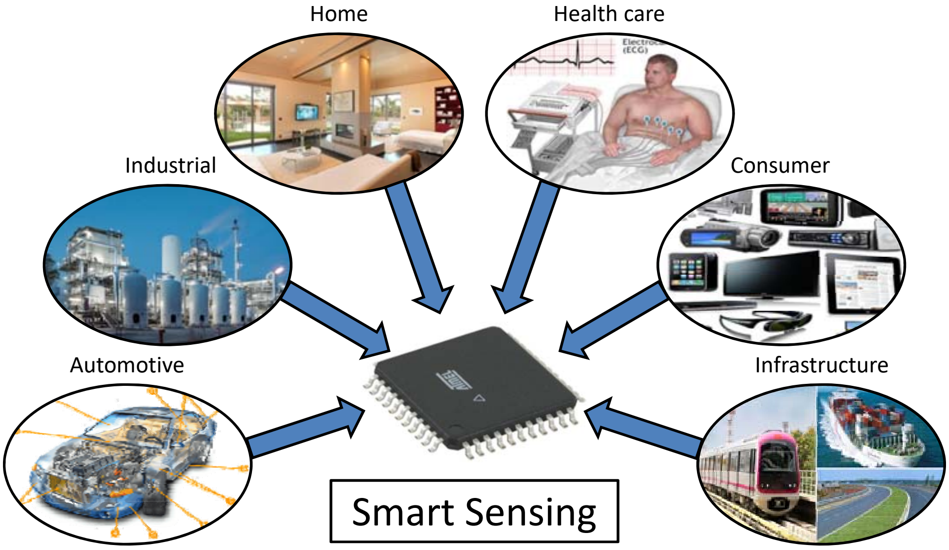
Abstract: The continuous progress of CMOS semiconductor technology fuels the technological revolution towards a smart world that immersively impacts our daily life, work and play. The Internet of Things, personalized healthcare monitoring, autonomous driving, industry 4.0, etc. are but a few examples. Sensors and sensor interfaces with intelligence in the edge play a key role in all applications where the physical and the cyber worlds meet. This presentation will focus on core challenges in the design of future electronic circuits for such applications, where cost, power and reliability are major issues besides raw performance. The key to achieve solutions with small area (cost) and low power is to design the analog functions in a highly digital manner. Also ways to build intelligence in the edge will be discussed. This will be illustrated with some practical design examples.

Biography: Georges G.E. Gielen (gielen@kuleuven.be) received his M.Sc. and Ph.D. degrees in electrical engineering from KU Leuven, Belgium, in 1986 and 1990, respectively. In 1990, he was a post-doctoral research assistant and a visiting lecturer with the Department of Electrical Engineering and Computer Science, the University of California Berkeley. Since 1991, he has worked in the MICAS research group with the Department of Electrical Engineering, KU Leuven, where he currently is a full professor. His research interests include computer-aided design of analog and mixed-signal ICs, including data converters and sensor readout circuits. He has authored or coauthored 10 books and more than 600 papers in edited books, international journals, and conference proceedings. He is Fellow of the IEEE and received the IEEE Circuits and Society Mac Van Valkenburg Award in 2015. He is a 1997 laureate of the Belgian Royal Academy of Sciences, Literature and Arts in the discipline of engineering.

Outline

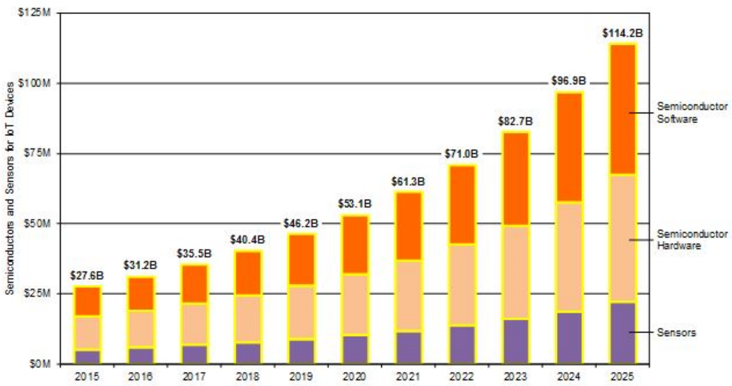
- **ubiquitous sensing in a smart world**
- how to make sensing small
- how to make sensing sound (robust)
- how to make sensing smart
- conclusions

Sensing is ubiquitous



IoT market forecasts

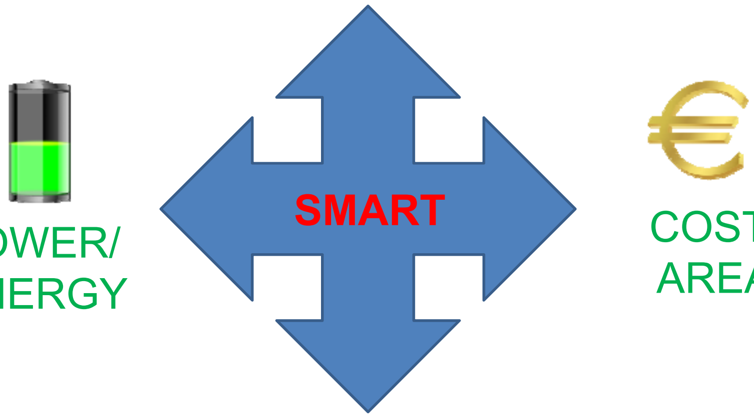
- expected growth from $46B in 2019 to $114B in 2025
  → CAGR = 15.3% >>> CAGR total semiconductor market



[semi.org 2015]

Requirements for sensing

PERFORMANCE



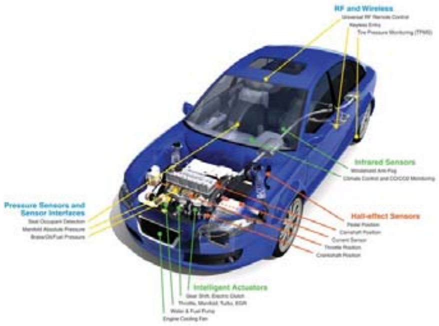
POWER/ ENERGY

COST/ AREA

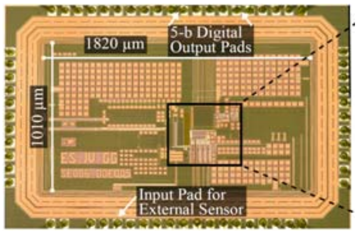
RELIABILITY/ROBUSTNESS

Automotive IC example

- automotive resistive sensor readout

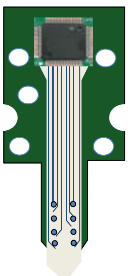


16.1 bit resolution
2nd/3rd–order noise shaping
highly-digital conversion
0.064 mm² in 0.18 µm CMOS

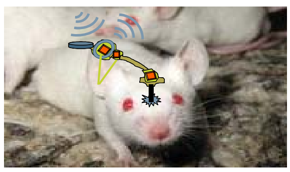


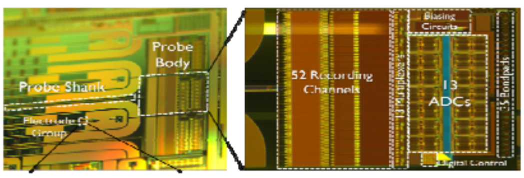
[Sacco ASSCC 2019 & JSSC 2020]

Biomedical IC example



- neural recording and stimulation
  - automatic closed-loop recording and stimulation
  - complete smart system with active probe and local processing



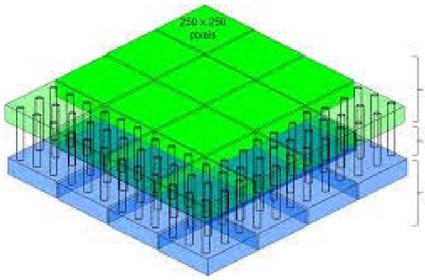


Shank : 1 cm by 100 µm
Probe body area is 2.9 mm × 3.3 mm
Read out 52 out of 455 electrodes
17.8 µW per channel
Plus : 13 stimulation electrodes

[Mora Lopez ISSCC 2013 & JSSC 2014]

Further miniaturization possible ?

- **example** : imagers with per-pixel readout
  - decouple resolution, SNR and frame rate
  - miniaturized cameras, e.g. artificial flying insects



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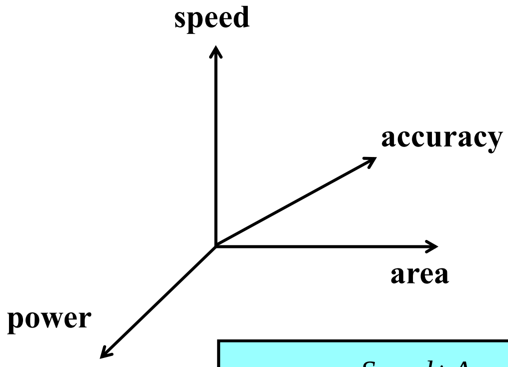
What makes analog circuits large ?



noise : [Vittoz ISCAS 1990]

$$P = 8kT\ f\ DR^2$$

mismatch :

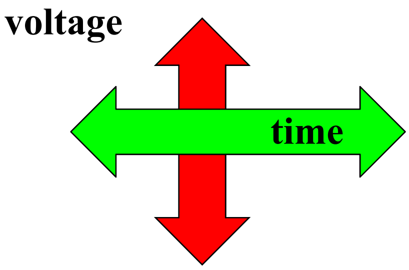
$$P = 24\, C_{ox}\, A_{VT}^2\ f\ DR^2$$

[Kinget CICC 1996]

$$\frac{Speed * Accuracy^2}{Power} = techn\,const$$

Towards digital-only analog circuits

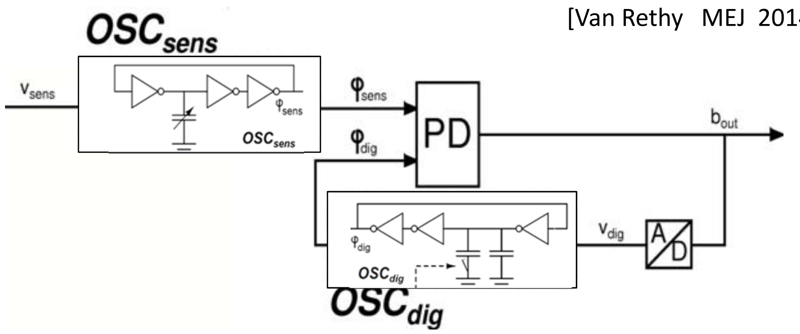
- **improve sensing performance and area :**
  exploit time/frequency processing
  ➔ exploits the improving CMOS timing resolution



➔ **solution : sensor to time/frequency to digital**

Time-based architecture

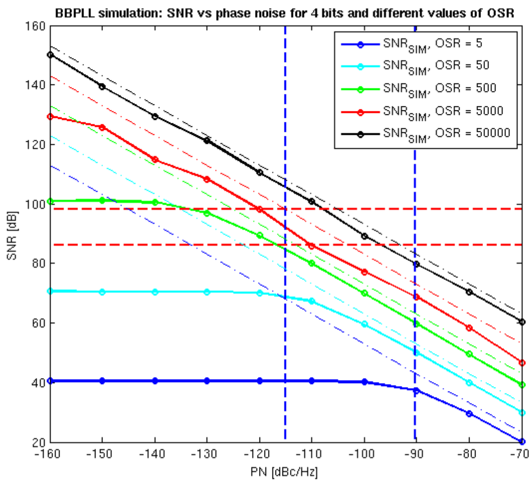
[Van Rethy MEJ 2014]



- highly-digital architecture → small area and scalable!
- use identically-implemented oscillators for modulation/de-modulation → robust conversion for common-mode errors
- ΔΣ similarity: noise shaping and oversampling possible !

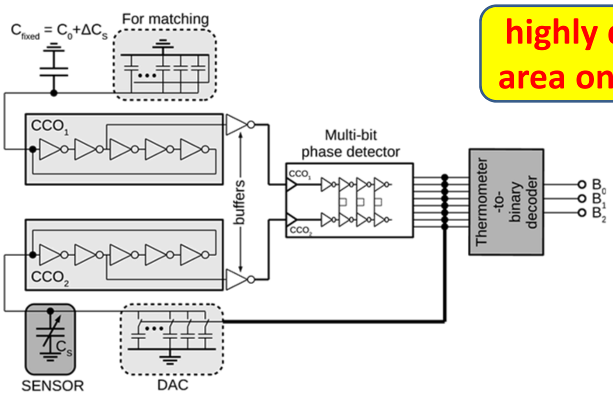
Performance limitation ?

- ultimately limited by phase noise or jitter of the VCOs

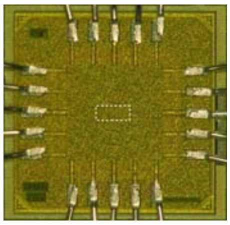


Capacitive time-based sensor interface

highly digital – active area only 0.0045 mm²

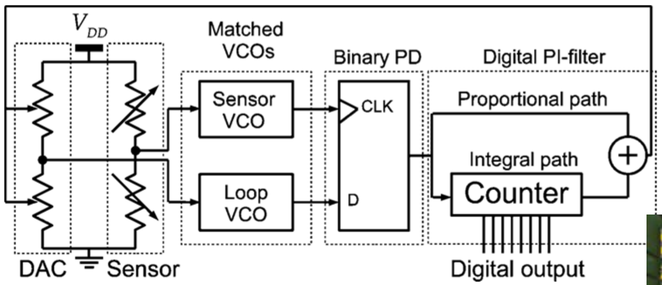


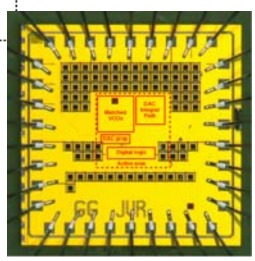
[Van Rethy MEJ 2014]



- first-order noise-shaping architecture
- 28 nm - **super-low-V_T transistors**: operated at **0.5 V**
- 5-stage **inverter** ring oscillators (cap-controlled)
- multi-bit phase detector
- active area = 108 µm x 42 µm = **0.00454 mm²**

Resistive time-based sensor interface



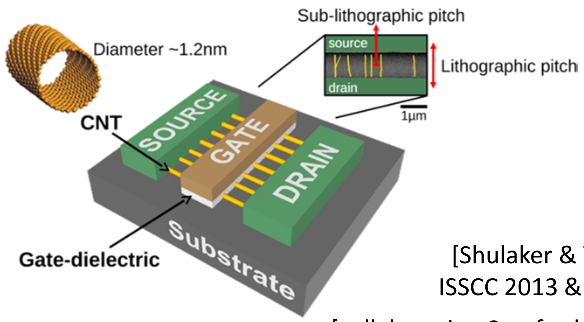


- force-balance the bridge
  - **2nd-order BBPLL** architecture
  - implicitly digitizes the sensor signal
    - sensor to digital conversion
- small area and technology scalable !
- implemented in 130 nm at 1V

[Van Rethy JSSC 2013]
[Van Rethy ASSCC 2012]

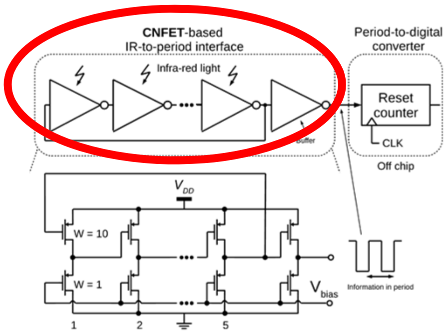
Use of emerging nanotechnologies

- **Carbon NanoTube (CNT)** technology is an excellent candidate
  - CNFETs are projected to improve in **energy-delay product with >10x** compared to Si CMOS at highly-scaled nodes
- CNTs are also ideal to be functionalized as **sensors**!
- have demonstrated several interface circuits

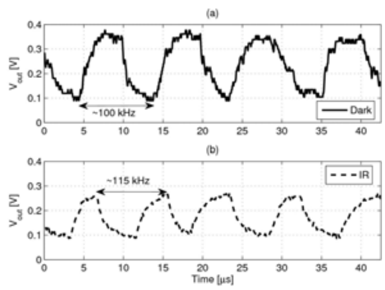


[Shulaker & Van Rethy ISSCC 2013 & JSSC 2014]
[collaboration Stanford U – KU Leuven]

Example: sensing with embedded IR



[Shulaker & Van Rethy ACS Nano 2014]



- oscillator functions as **infrared sensor**
  - inverters sensitive to infrared
- for 32 nm CNT: **100 kHz** range, **power only 130 nW**

How to achieve ultra-miniaturization ?

- **implement digital-like** where possible
  - avoid analog to implement analog functions
- **exploit time** / oversampling / averaging…
- use **advanced nanotechnologies**
  - CMOS, CNT…
  - use the 3rd dimension : 3D stacking
- **exploit the system level**
  - redundancy / sensor fusion
  - exploit signal characteristics / information features…
- …

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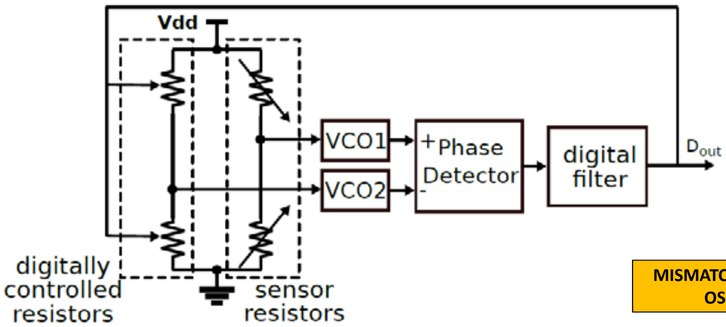
How to make it robust and resilient ?



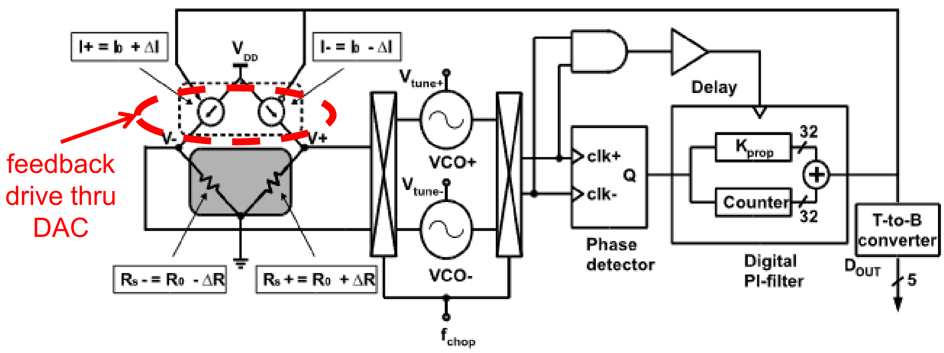
MISMATCH BETWEEN VCO OSCILLATORS

SUPPLY VARIATIONS

EXTENDED TEMPERATURE RANGE: -40°C to 175°C

CIRCUIT DEGRADATION / AGEING AND PACKAGE STRESS VARIATION: 10000+ HOURS OF RELIABLE OPERATION

Low-drift current feedback architecture



- temperature-stable transfer function, insensitive to **common-mode errors**

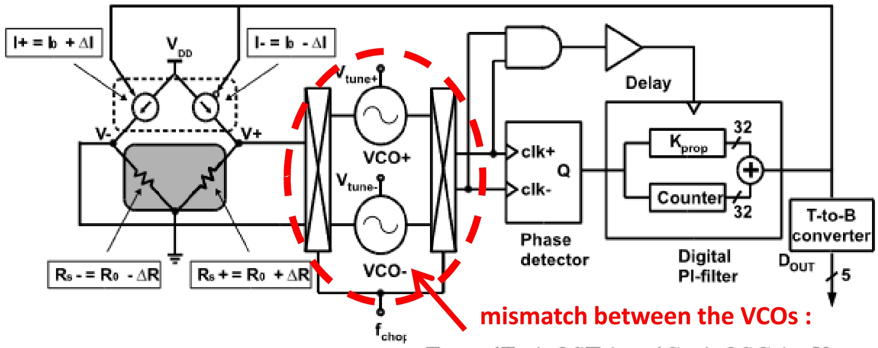
$$\frac{\Delta R}{R_0} = \frac{I_{LSB}}{I_0} \cdot D_{OUT}$$

ideal transfer function

[Marin ESSCIRC 2018 & JSSC 2019]

Time-based chopping

[Marin ESSCIRC 2018 & JSSC 2019]

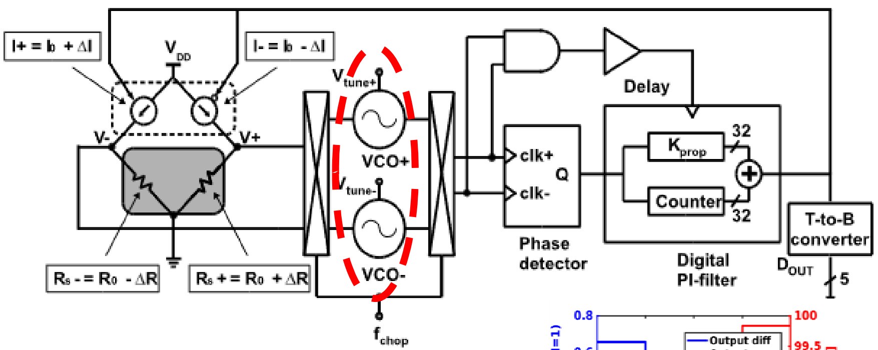


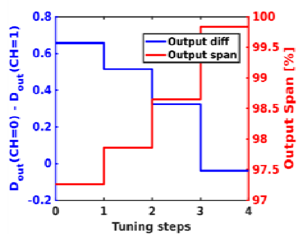
$$T_{\pm} = (T_0 \pm \mathrm{OST}_0) + (G_1 \pm \mathrm{OSG}_1) \cdot V_{\mathrm{eff}\pm} + (G_2 \pm \mathrm{OSG}_2) \cdot V_{\mathrm{eff}\pm}^2 + \ldots$$

- chopping removes impact of DC (offset) and low-frequency (1/f noise) errors, but not completely if both frequency and gain mismatch error exist

VCO tuning

[Marin ESSCIRC 2018 & JSSC 2019]

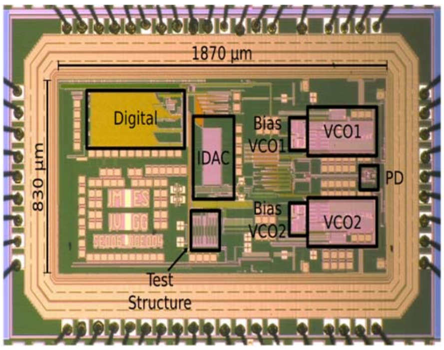


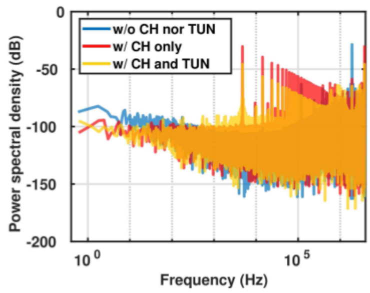


- VCO bias current tuning eliminates the remaining error
- low-overhead technique
- no accurate reference nor external components needed

Robust 0.18µm CMOS readout chip

[Marin ESSCIRC 2018 & JSSC 2019]

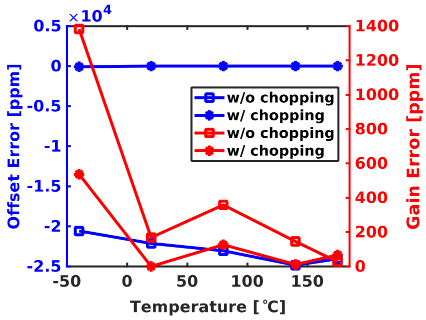




- 15.0 ENOB achieved with chopping and tuning

Robust 0.18µm CMOS readout chip

[Marin ESSCIRC 2018 & JSSC 2019]



EXTENDED TEMPERATURE RANGE: -40°C to 175°C

- ultra low temperature drift due to combination of current steering of the bridge, chopping and VCO tuning
  - 0.3 ppm/°C for offset and 2.3 ppm/°C for gain

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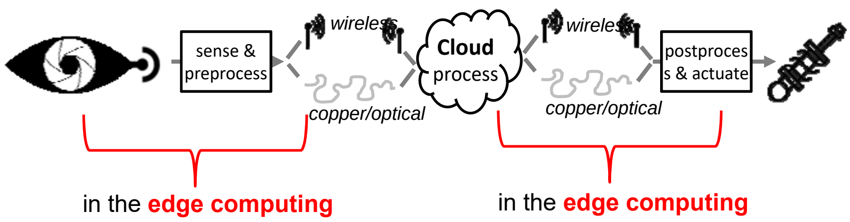
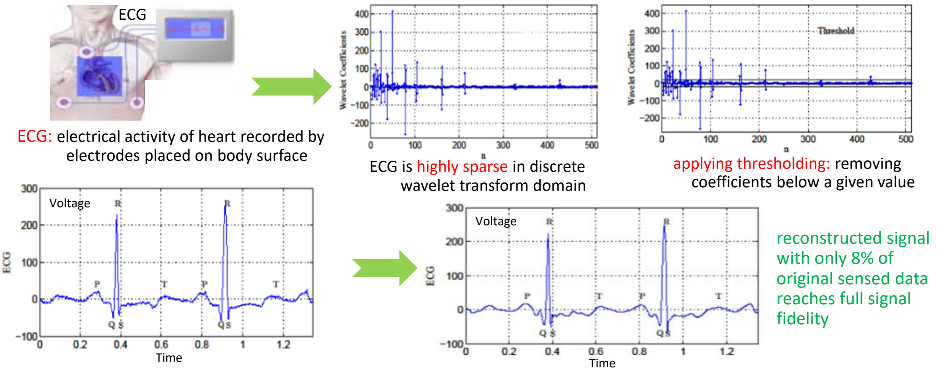
Smart system architecture



- dynamically adaptive performance scaling
- bio-inspired sensing and read-out :
  - only sample signal when there is information
    → event-based sensing
  - only sample the relevant information
    → embedded signal compression / feature extraction
    → smart and compressive signal encoding
- embed (autonomous) learning at the edge

Compressed sensing

- sensing is the dominant energy cost in biosignal analysis
  - more than 80% in sampling, while 7% in processing and 13% in communication



- development of compressed sensing and processing for biosignals
  - large power savings possible [Mamaghanian TBioEng 2011 & JESTCAS 2012]

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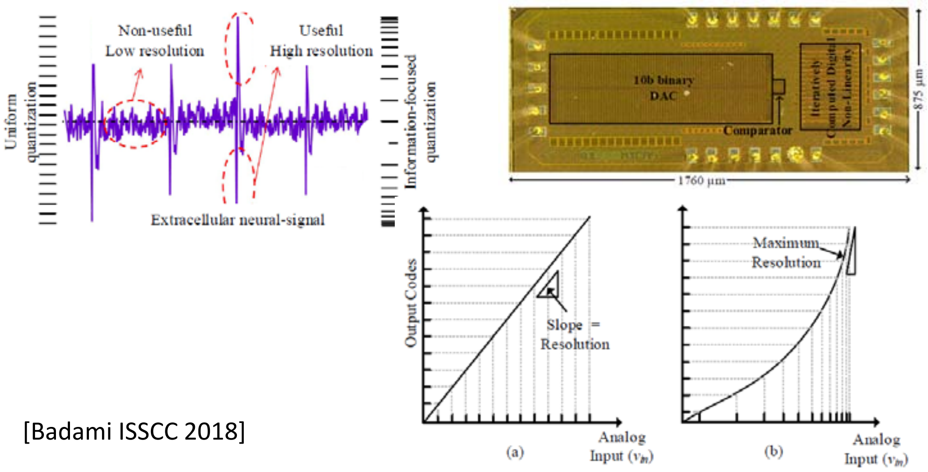
Signal-dependent processing

– concept : only sample the relevant information
→ embedded signal compression / feature extraction



[Badami ISSCC 2018]

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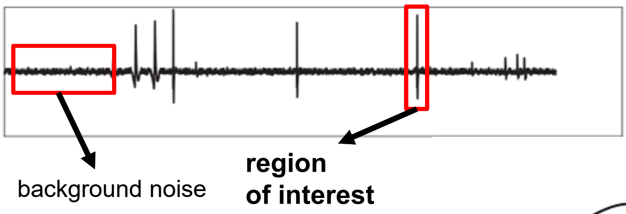
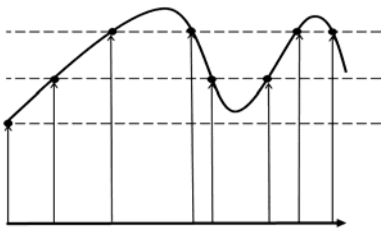
Event-based sensing

– concept: only sample when there is relevant information
→ embedded signal compression / feature extraction

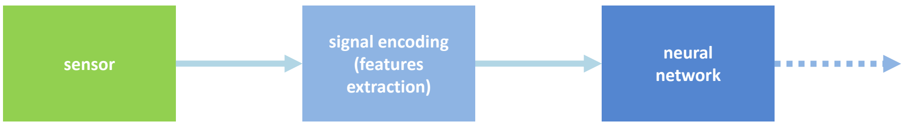


event-based asynchronous sampling

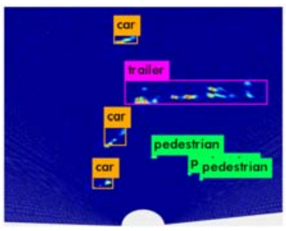


Cognitive sensing

- add features extraction and neural network for interpretation in the edge



- illustrative example : object recognition



Conclusions

- **networked sensing** has become ubiquitous
  - Internet of Things, personalized medicine, etc. as key drivers
- need for **miniaturized sensor interfaces**
  - highly digital architectures – small area - scalable
  - high power efficiency
- need for **ultra-reliable electronics**
  - extreme reliability
  - low drift – high resilience
- need for **intelligent edge computing**
  - embedded information extraction in the edge
  - fully adaptive processing with learning capability
  - exploit system-level redundancy with “simple” nodes

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- many thanks to all funding organisations: KU Leuven DOC, Flemish FWO, Flemish IWT/VLAIO, EU and the many companies supporting the research

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