More than Moore Analog Electronics for Harsh Environment Applications

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Who we are?
What we do research in Electronics?

More than Moore Analog Electronics for Harsh Environment Applications
Content

• Why do we need Research in Electronics?

• How do we do Research in Electronics?

• Research Trend Topics
  • More than Moore Analog Electronics
  • Electronics for Harsh Environments

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Industrial Revolution

- **Industry 3.0**
  - Processes Automation using electronics and information technology

- **Industry 4.0**
  - Smart and Green Industry – a **1.3 billion dollars** worldwide investment
Moore’s Law


Integration density versus time
Integrated circuits market

Theoretical limit: 8-12 nm

http://www.computerhistory.org/

20 k transistors
Intel 8086 – 1978
3 µm

3.1 M transistors
Intel Pentium - 1993
0.35 µm

1.6 B transistors
PlayStation 3 - 2006
90 nm

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More Moore and Beyond


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Electronics Economy

** AMD’s Most Advanced Mobile Processor **

- **Intel 22 nm (2013)**
- **Intel 14 nm (2014)**
- **Intel 14 nm (2015)**
- **Intel 14 nm (2016)**
- **Intel 14 nm (2017)**
- **AMD Ryzen™ Processor**
  - With Radeon™ Vega Graphics
  - 10/2017

- **TSMC 7 nm (2017)**
  - Power -30%
  - Performance +15%
  - 2020

- **TSMC 5 nm (2022)**
  - Power -25%
  - Performance +10%

** More than Moore Analog Electronics for Harsh Environment Applications **
Industrial Revolution 4.0

- Internet-of-Things (IoT) are introducing new power and decision autonomous electronics in consumer products

**Needs:**
- Ultra-low power
- AI-edge
- Real time
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Electronics – Hierarchical Discipline

\[ A_v \geq 2^{\text{bits}} \]
\[ P_{\text{tot}} \leq 100 \, \text{mW} \]
\[ P_{\text{DC}} = I_D \cdot V_{DD} \]
\[ A_v = g_m \cdot R_L \]
\[ g_m/I_D = f_T \]
\[ g_m/g_{DS} = f_{CO} \]

BSIM6, PSP, UICM

\[ I_D = \eta g_m \phi_t \left[ 1 + \frac{g_m}{2\mu_n C_{ox} \phi_t(W/L)} \right] \]
SiN Passivation Layer

Process Level – SOI Technology

- Metal alloy & high-k insulators – high speed passive devices
- SiO$_x$N$_y$ oxide
- SiO$_2$ oxide

Nanometric transistors – high integration

- SOI – low leakage current

- Modelling – BSIM6, PSP, UICM

Si Substrate P-
Transistor Level – from Weak to Strong inversion MOSFET

Weak inversion (WI)

\[ I_{WI} = I_S e^{\frac{V_{GS}}{\eta \phi_t}} \quad \rightarrow \quad I_{WI} = \eta g_m \phi_t \]

Strong inversion (SI)

\[ I_{SI} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 \quad \rightarrow \quad I_{SI} = \frac{ng_m^2}{2\mu_n C_{ox} \left( \frac{W}{L} \right)} \]

\( V_{th} \) is the threshold voltage at \( V_{SB} = 0 \), \( \frac{W}{L} \) is the geometric ratio, \( \mu_n \) is the mobility, \( n \) is the slope factor (from 1.1 to 1.5), and \( C_{ox} \) is the oxide capacitance per unit area.
Transistor Level – All-region “interpolation” model

\[ I_{WI} = \eta g_m \phi_t \quad \text{interpolation} \quad I_{SI} = \frac{n g_m^2}{2\mu_n C_{ox} (W/L)} \]

For \( g_m \to \infty \), \( I_{WI} \) is negligible; while for \( g_m \to 0 \), \( I_{SI} \) is negligible

\[ I_D = I_{WI} + I_{SI} = \eta g_m \phi_t \left[ 1 + \frac{g_m}{2\mu_n C_{ox} \phi_t (W/L)} \right] \]

\[ I_D = I_{WI} \left[ 1 + \frac{(W/L)_{th}}{(W/L)} \right] \leftrightarrow g_m = 2\mu_n C_{ox} \phi_t (W/L)_{th} \]

where \((W/L)_{th}\) is the normalized aspect ratio
Transistor Level – The Unified Current Control Model (UICM)

\[ g_{ms} = \frac{\partial I_D}{\partial V_S}, \quad g_m = \frac{\partial I_D}{\partial V_G} \quad \therefore \quad g_m = \frac{g_{ms}}{\eta} \]

\[ g_{ms} = \frac{\partial I_D}{\partial V_S} = -I_s \frac{\partial i_f}{\partial V_S} = \frac{2I_s}{\phi_t} \left( -1 + \sqrt{1 + if} \right) \]

\[ -\frac{V_T}{2} \frac{\partial i_f}{\partial V_S} = \partial V_S \]

\[ V_P - V_S = \phi_t \left[ \sqrt{1 + if} - 2 + \ln \left( -1 + \sqrt{1 + if} \right) \right] \]

\[ V_P = \frac{V_G - V_{th}}{\eta} \quad \text{\(V_P\) (pinch-off voltage) comes from the channel length modulation effect} \]

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Circuit Level – $g_m/I_D$ Methodology

- Black box approach
- Design of Experiments
- Intuitive Design

\[
\eta g_m \phi_t \frac{1}{I_D} = \frac{2}{1 + \sqrt{1 + if}}
\]

\[
g_m \frac{1}{I_D} = \frac{2}{\eta \phi_t (1 + \sqrt{1 + if})}
\]

Circuit Level – Find the best Trade-off

- EDA Optimization problems

\[ P = V_{DD} \cdot \sum I_D \]
\[ J_{DS} = \frac{I_D}{W} \]
\[ S = L \cdot \sum W_i \]

### Power

\[ W_I \]
\[ M_I \]
\[ S_I \]

### Gain

\[ A_V = -\frac{g_m}{g_{DS}} \]

### Speed

\[ f_T = \frac{g_m}{2 \pi (C_{GS} + C_{GD})} \]

### Noise

\[ f_{CO} = \frac{K_f}{C_{ox} L} \cdot \frac{g_m}{I_D} \cdot \frac{J_{DS}}{4kT\gamma} \]

\[ \frac{GBW}{SR} = \frac{g_m}{I_D} \]


System Level – Hybrid ADCs

- Novel Topologies as hybrid and heterogeneous solutions
- Performance constraint share
  - Faster, higher resolution and low power

System Level – MEMS instrumentation

Mechanical
(M. Gouspy)

Electronics
( João R. R. O. Martins)

\[ x(t) = X \sin(\Omega t + \phi) \]

Resonator X
\[ K \times (1 + \varepsilon), \gamma, Q, \alpha \]

Converter
(A. Mostafa)

\[ \sum \Delta \]

\[ \phi = \frac{\pi}{2} \cdot (1 + 2Q\varepsilon) \]

Unreliable Electronics

\[ \phi = \frac{\pi}{2} \cdot \left( 1 + 2Q \left( \varepsilon + \frac{\sqrt{2}}{2Q} \cdot \Delta \theta \right) \right) \]


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More than Moore: Silicon in Photonics

- Better data transmission – Light is not bounded to wire connection limitations (8 Gbps for PCIe)
- Higher integration costs – Requires a SiP post processing
- Smaller footprint – Computer Motherboard in a single ASIC
A 0.9 pJ/bit, low-ER SiP transmitter

- Heterogenous SiP solution
  - bond wires connection
- System-level Optimization
  - Power consumption
  - Extinction Ratio reduction
- 20 Gbps data rate

Ph.D. A. Michard solution

1 segment MZM of 824 µm
ER = 0.73 dB
20 Gbps
0.9 pJ/bit


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More than Moore: Artificial Intelligence

- **Biological Solutions**
  - Ion charge conduction
  - Living cells

- **Software Solutions**
  - Binary based
  - Von Neumann Computer

### Biological Neuron

- **Synapses**
- **Dendrites**
- **Nucleus**
- **Axon**

- **Membrane**
  - $[K^+] = 160\, \text{mM}$
  - $[Na^+] = 144\, \text{mM}$

- **Channels**
  - $K^+$ and Na$^+$

- **Axon Terminals**
  - $E_{Na} = +60\, \text{mV}$
  - $E_K = -90\, \text{mV}$

### Artificial Neuron

- **Σf**
- **Bias**
- **Hyperbolic Tangent**

- **Input Layer**
- **Hidden Layer**
- **Output Layer**
Neuromorphic Analog Spiking-Modulator
a 55 nm Integrated SNN solution

- Analog Hardware Solutions
  - Neuron model validated
  - Lack of plasticity in synapses


NASP: 9 bits de resolution, 8 fJ/conv


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Harsh Environments: Radiation and Aging

- Failure is increasing in nanometric electronics
- Transistor lifetime below few years!

Transistor-level: Reliability Resilience

- Modeling HCI and NBTI of ST 65 nm
- Enable a $g_m/I_D$ methodology
- Negligible aging – reliable design space


System-Level: Faulty building blocks

- Continuous Time $\Sigma\Delta$ ADC
- Building block failure tests
  - OpAmp Failure
    - Gain drop
    - GBW limitation
  - Clock
    - Skew
    - Jitter

Harsh Environments: High Temperature

- Smart Vehicles – efficiently sense and communicate with other nearby devices
- Safety in working environment – high temperature
- Low costs – use standard processes, digital-enabled

More than 200 sensors expected
Harsh Environments: High Temperature

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$T_{\text{max}} = 250 \, ^\circ\text{C}$

$T_{\text{max}} = 175 \, ^\circ\text{C}$

$T_{\text{max}} = 125 \, ^\circ\text{C}$
$g_m/I_D$ Methodology fails in high temperature

\[ g_m/I_D = \frac{1}{\phi_e} \frac{2}{\eta(V_G)(q_{is}(V_G, V_S) + q_{id}(V_G, V_S) + 2)} \]

Temperature Dependency

$\eta(V_G)(q_{is}(V_G, V_S) + q_{id}(V_G, V_S) + 2)$

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Temperature Aware $g_m/I_D$ Methodology

J. R. R. O. Martins, Ph.D. cand methodology

Temperature Normalized Parameter

Temperature Aware OTA

Ph.D. A. Mostafa design

<table>
<thead>
<tr>
<th>Device</th>
<th>$g_m/I_d$</th>
<th>To minimize</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_0$</td>
<td>6</td>
<td>$S_{IDS}^T$</td>
</tr>
<tr>
<td>$M_{1(2)}$</td>
<td>9</td>
<td>$S_{g_m}^T$</td>
</tr>
<tr>
<td>$M_{3(4)}$ and $M_{5(6)}$</td>
<td>5 ($L = 3\mu m$)</td>
<td>$S_{IDS}^T$ and $S_{g_{ds}}^T$</td>
</tr>
<tr>
<td>$M_{7(8)}$ and $M_{9(10)}$</td>
<td>6 ($L = 3\mu m$)</td>
<td>$S_{IDS}^T$ and $S_{g_{ds}}^T$</td>
</tr>
</tbody>
</table>
Thank you very much