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More than Moore Analog Electronics for Harsh Environment Applications

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Université Paris-Saclay, CentraleSupélec

cnrs dépasser les frontières

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Who we are?

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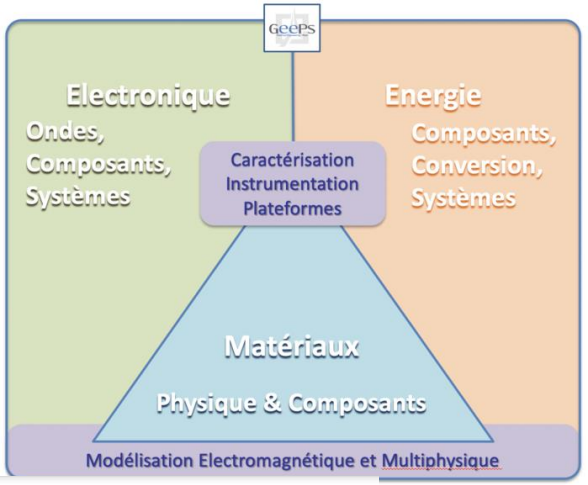
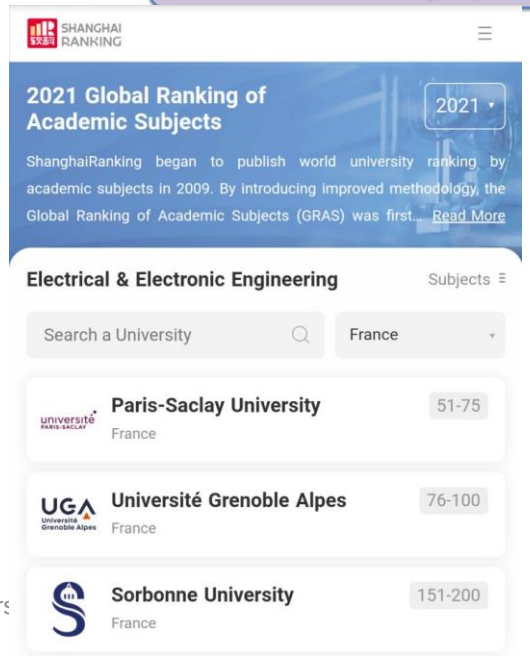
Plateau de Saclay

Université Paris-Saclay





What we do research in Electronics?

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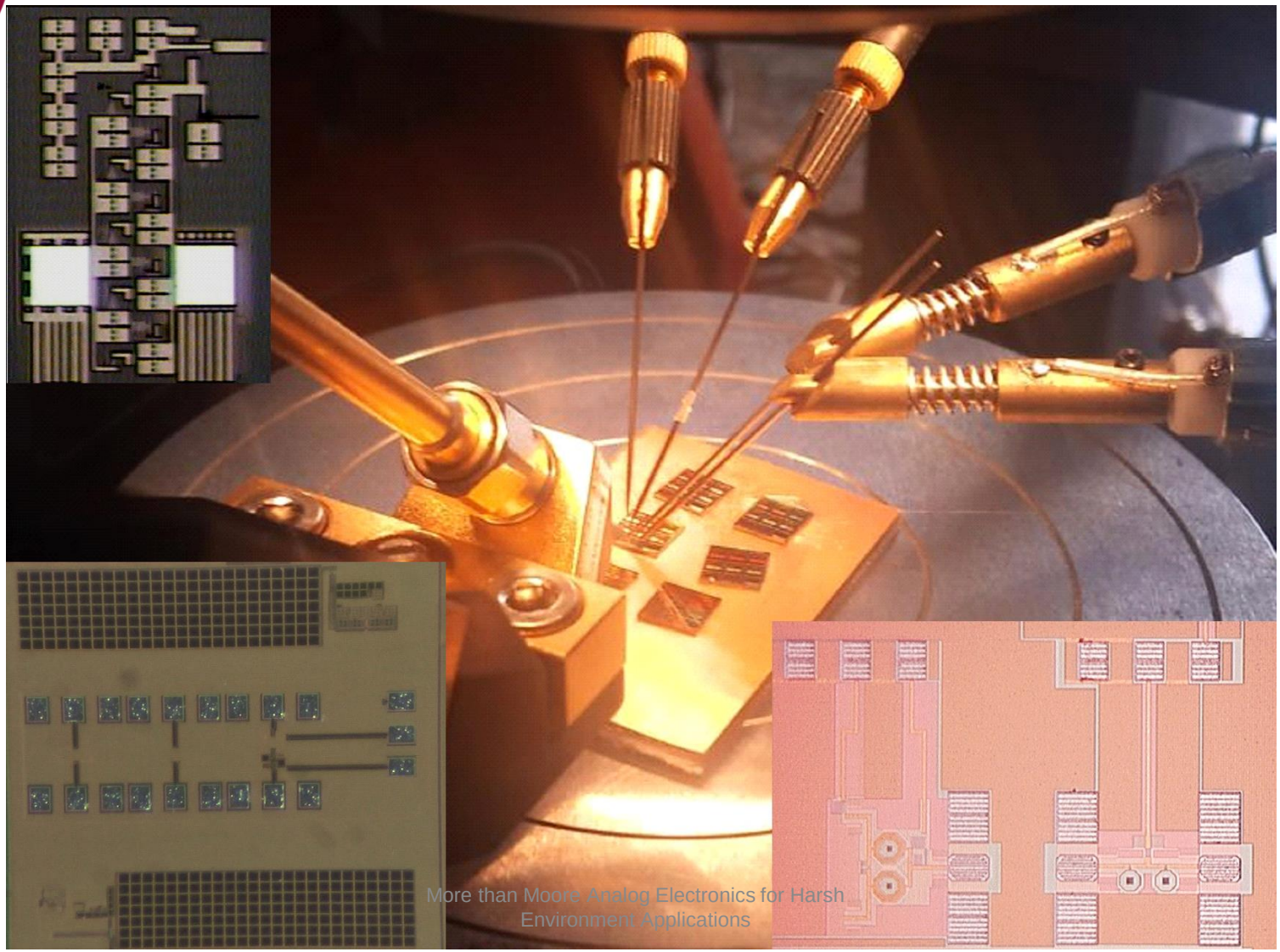

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Content

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- Why do we need Research in Electronics ?
- How do we do Research in Electronics ?
- Research Trend Topics
  - More than Moore Analog Electronics
  - Electronics for Harsh Environments

Industrial Revolution

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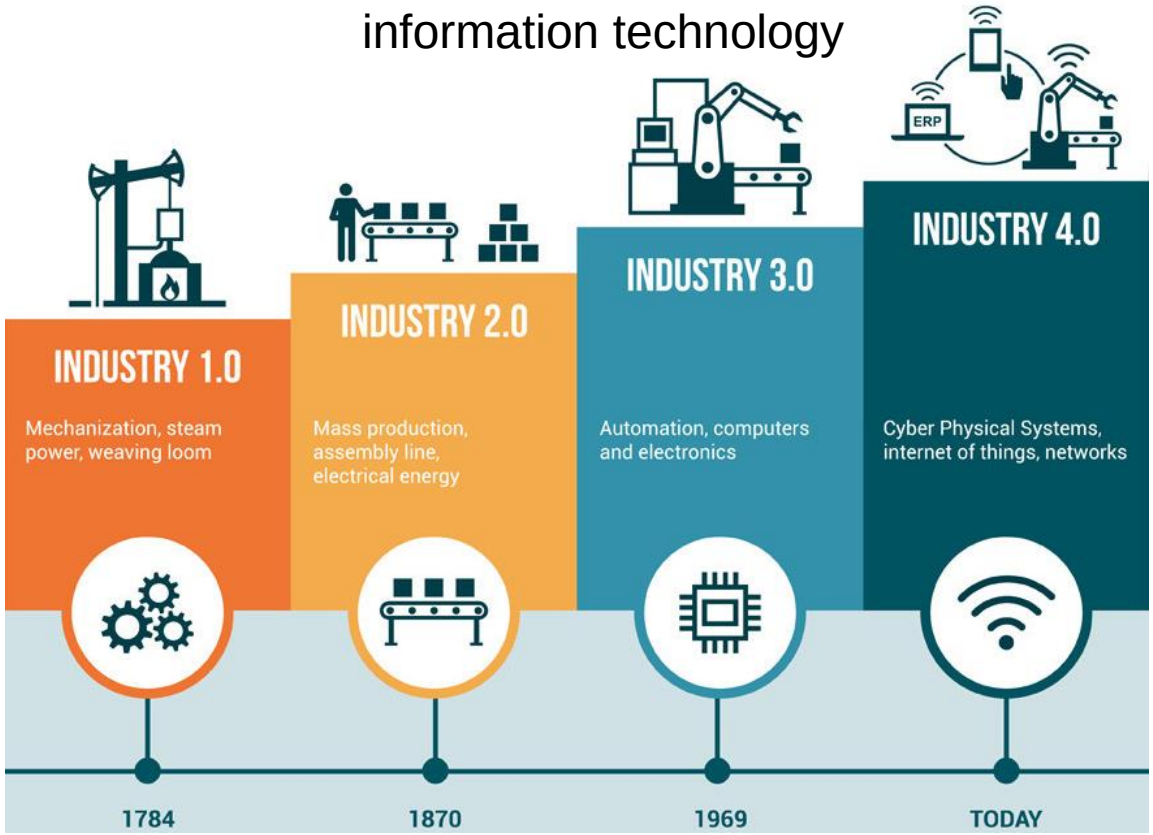
- Industry 3.0
  - Processes Automation using electronics and information technology

- Industry 4.0
  - Smart and Green Industry – a **1.3 billion dollars** worldwide investment



Moore's Law

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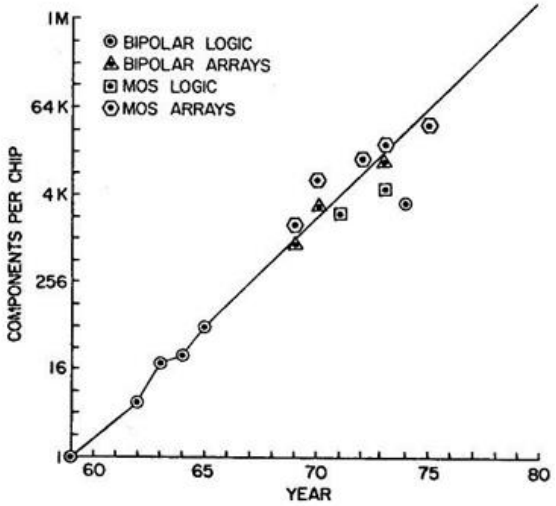
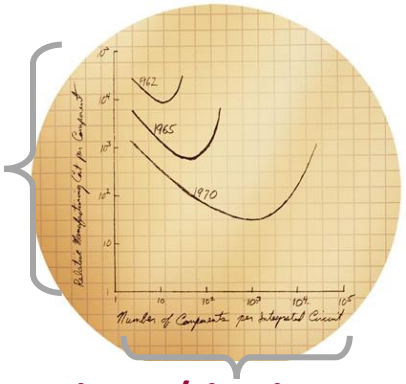
1965: Moore's Law: **Prediction** of future of integrated circuits

Integration density versus time

Integrated circuits market

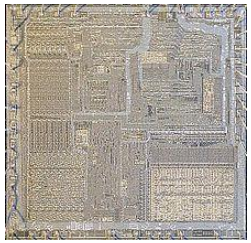


$/circuit

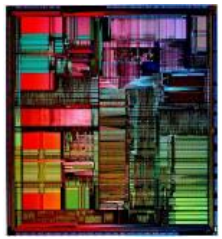


 # transistors/circuit

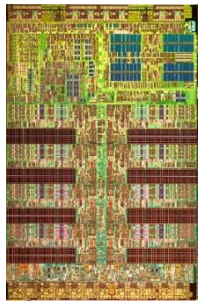
Theoretical limit: 8-12 nm



20 k transistors
Intel 8086 – **1978**
3 µm



3.1 M transistors
Intel Pentium - **1993**
0.35 µm



1.6 B transistors
PlayStation 3 - **2006**
90 nm

Source:
D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proc. IEEE*, vol. 89, no. 3, pp. 259–287, 2001.
http://www.computerhistory.org/
http://www.tayloredge.com/museum/processor/processorhistory.html

More Moore and Beyond

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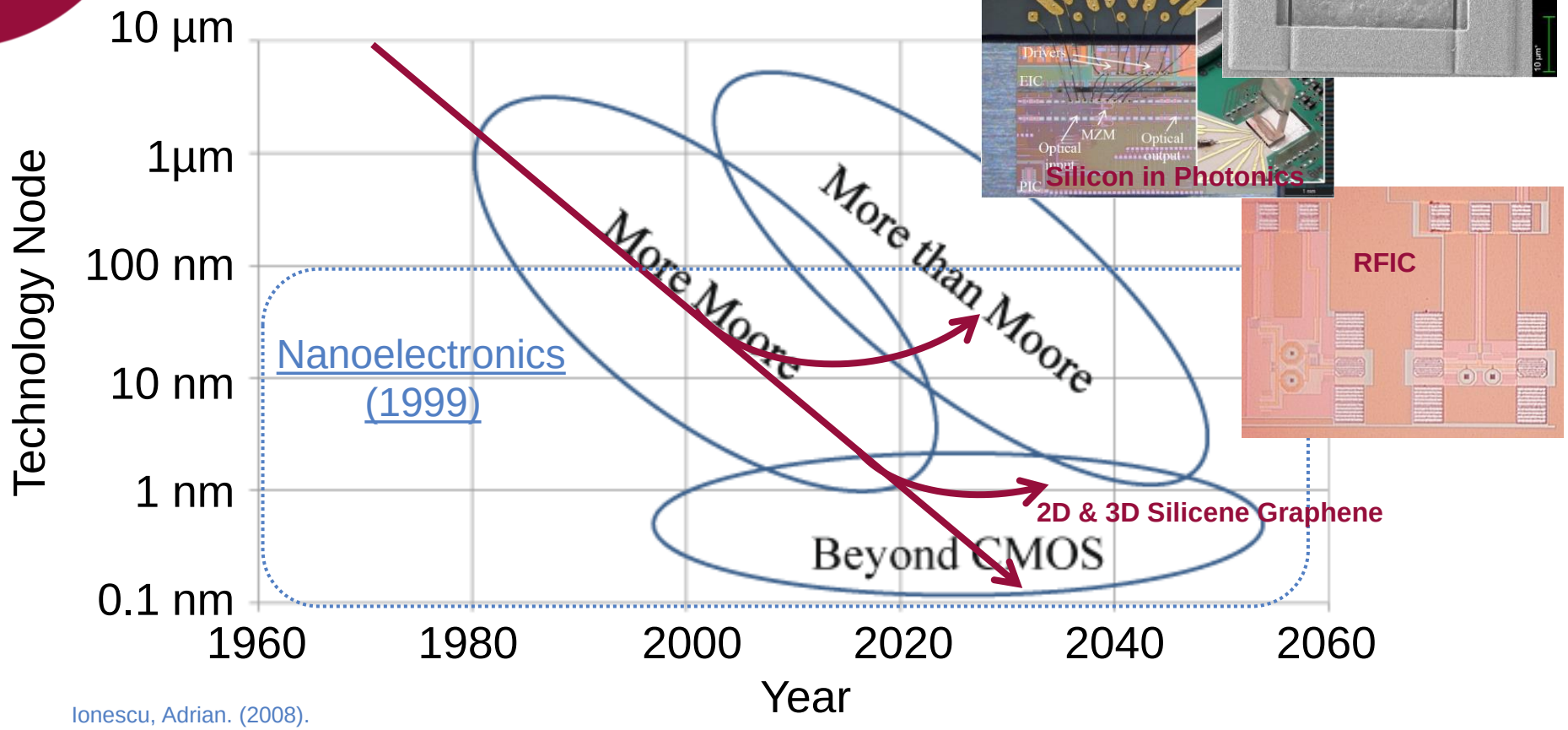

Ionescu, Adrian. (2008). Nanoelectronics roadmap: evading Moore's law.

Electronics Economy

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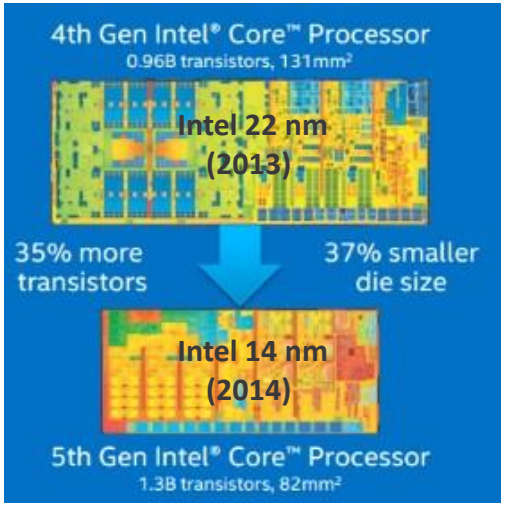
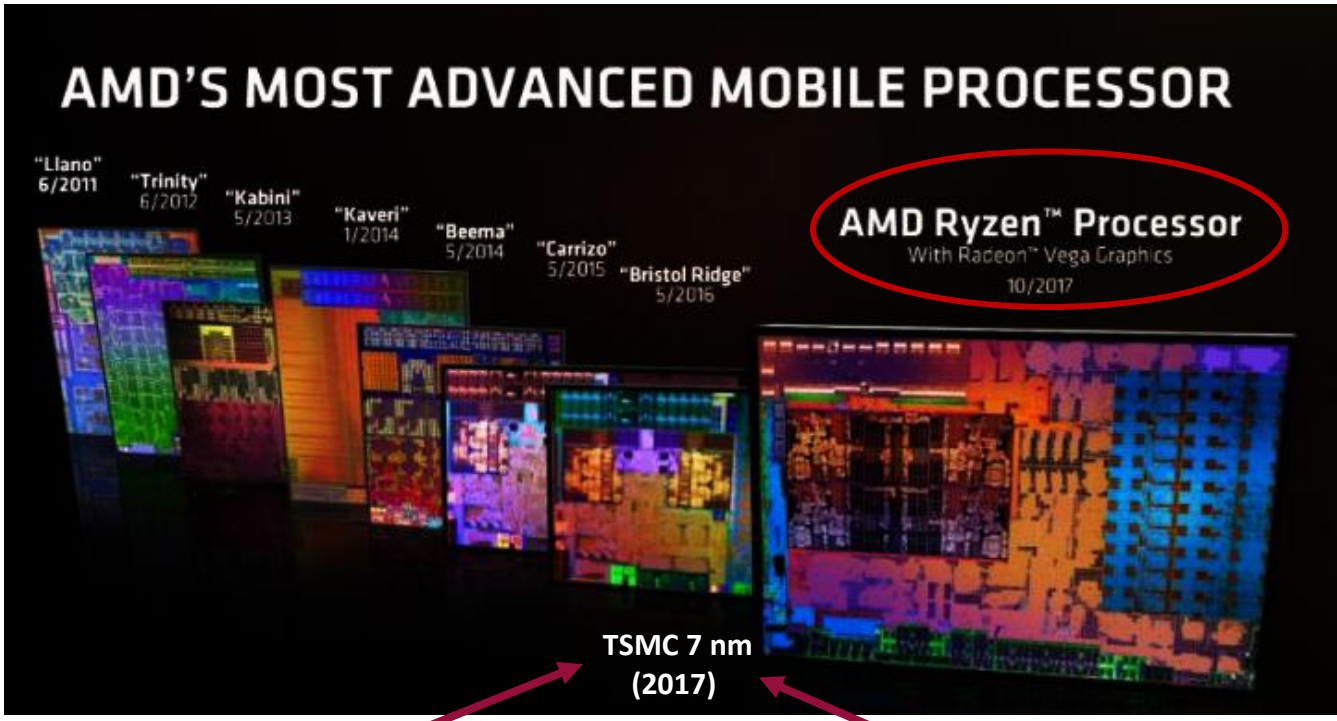
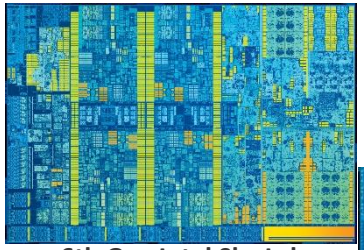
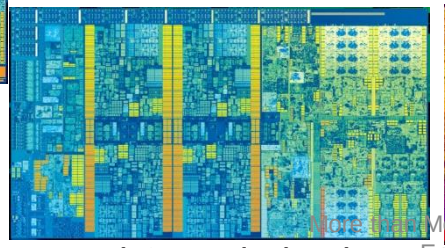






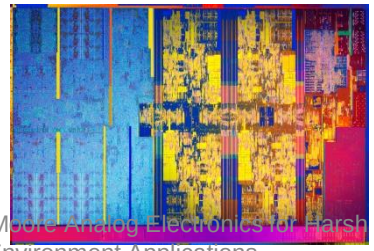
6th Gen Intel Sky Lake
Intel 14 nm
(2015)

Intel 14 nm
(2016)

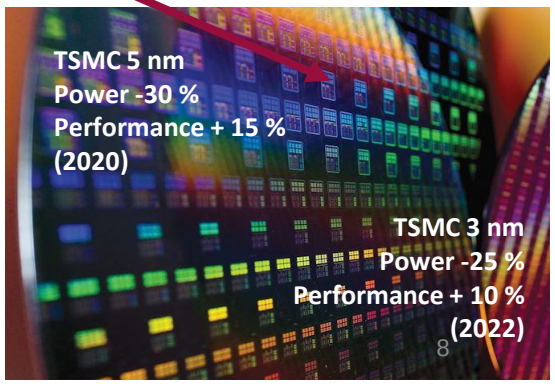


7th Gen Intel Kaby Lake

Intel 14 nm
(2017)



8th Gen Intel Coffee Lake



Industrial Revolution 4.0

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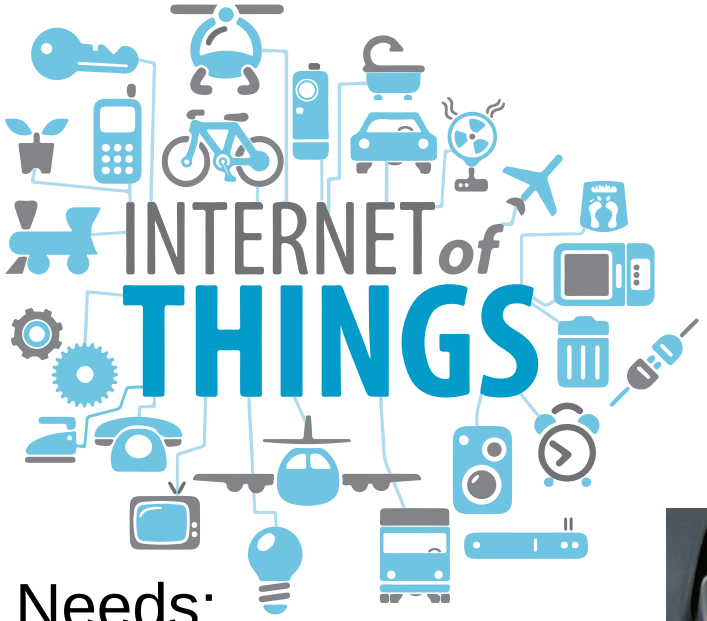
- Internet-of-Things (IoT) are introducing new power and decision autonomous electronics in consumer products



- Needs:
  - Ultra-low power
  - AI-edge
  - Real time

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Electronics – Hierarchical Discipline

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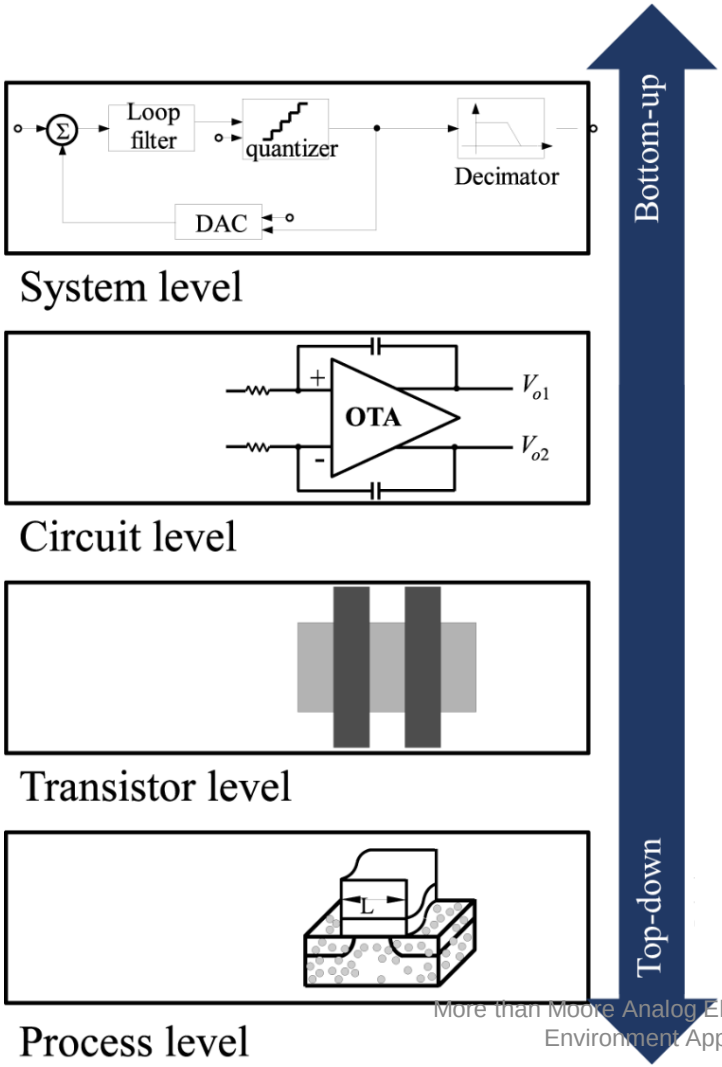


$$A_v \geq 2^{bits}$$

$$P_{tot} \leq 100\,mW$$

$$P_{DC} = I_D \cdot V_{DD}$$

$$A_v = g_m \cdot R_L$$

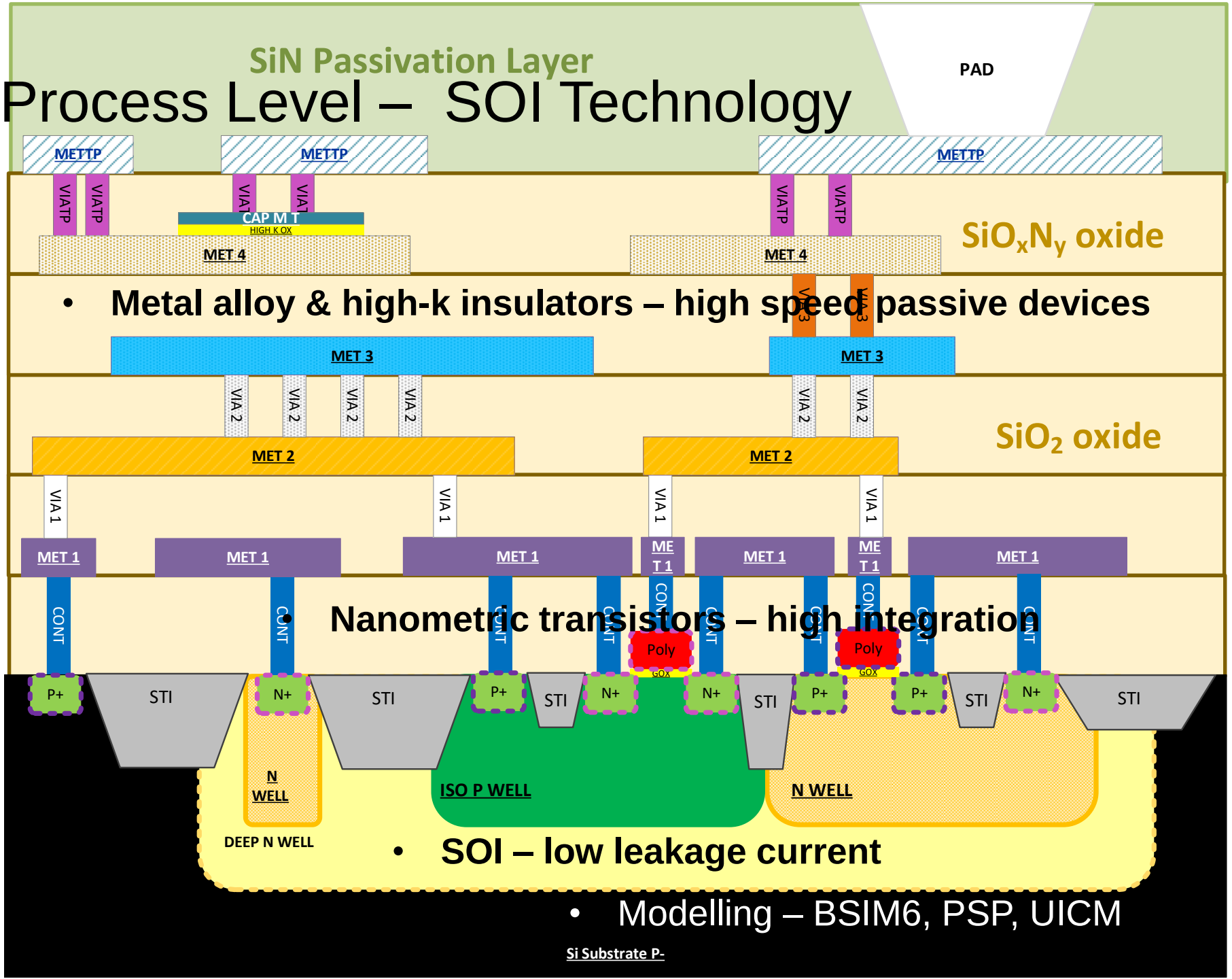
g_m/I_D f_T

g_m/g_{DS} f_{CO}

BSIM6, PSP, UICM

$$I_D = \eta g_m \phi_t \left[1 + \frac{g_m}{2\mu_n C_{ox} \phi_t (W/L)}\right]$$

Process Level – SOI Technology



Transistor Level – from Weak to Strong inversion MOSFET

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Weak inversion (WI)

$$I_{WI} = I_S e^{V_{GS}/\eta\phi_t} \longrightarrow I_{WI} = \eta g_m \phi_t$$

Strong inversion (SI)

$$I_{SI} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2 \longrightarrow I_{SI} = \frac{n g_m^2}{2\mu_n C_{ox}(W/L)}$$

V_{th} is the threshold voltage at $V_{SB} = 0$, W/L is the geometric ratio, μ_n is the mobility, is n the slope factor (from 1.1 to 1.5), and C_{ox} is the oxide capacitance per unit area

Transistor Level – All-region "interpolation" model

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$$I_{WI} = \eta g_m \phi_t \xrightarrow{\text{interpolation}} I_{SI} = \frac{n g_m^2}{2\mu_n C_{ox} \left(W/L\right)}$$

For $g_m \to \infty$, I_{WI} is negligible; while for $g_m \to 0$, I_{SI} is negligible

$$I_D = I_{WI} + I_{SI} = \eta g_m \phi_t \left[1 + \frac{g_m}{2\mu_n C_{ox} \phi_t \left(W/L\right)}\right]$$

$$I_D = I_{WI}\left[1 + \frac{\left(W/L\right)_{th}}{\left(W/L\right)}\right] \leftrightarrow g_m = 2\mu_n C_{ox} \phi_t \left(W/L\right)_{th}$$

where $\left(W/L\right)_{th}$ is the normalized aspect ratio

Transistor Level – The Unified Current Control Model (UICM)

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$$g_{ms} = \frac{\partial I_D}{\partial V_S}, g_m = \frac{\partial I_D}{\partial V_G} \therefore g_m = \frac{g_{ms}}{\eta}$$

$$g_{ms} = \frac{\partial I_D}{\partial V_S} = -I_S \frac{\partial if}{\partial V_S} = \frac{2I_S}{\phi_t}\left(-1 + \sqrt{1 + if}\right)$$

$$-\frac{V_T}{2} \frac{\partial if}{\left(-1 + \sqrt{1 + if}\right)} = \partial V_S$$

$$V_P - V_S = \phi_t\left[\sqrt{1 + if} - 2 + ln\left(-1 + \sqrt{1 + if}\right)\right]$$

$$V_P = \frac{V_G - V_{th}}{\eta}$$

V_P (pinch-off voltage) comes from the channel length modulation effect

C. Galup, M. Schneider, and I. Si, “The compact all-region MOSFET model : theory and applications,” in *IEEE New Circuits Syst. Conf.*, 2018, pp. 166–169.

Circuit Level – g_m/I_D Methodology

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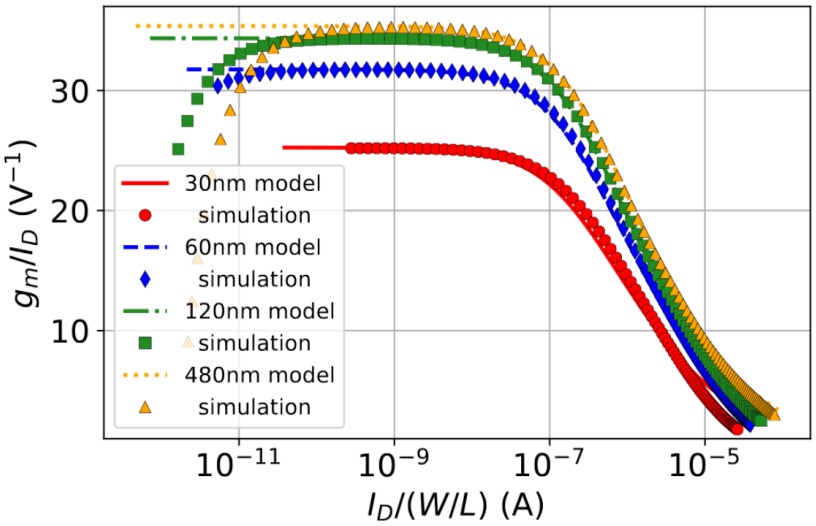
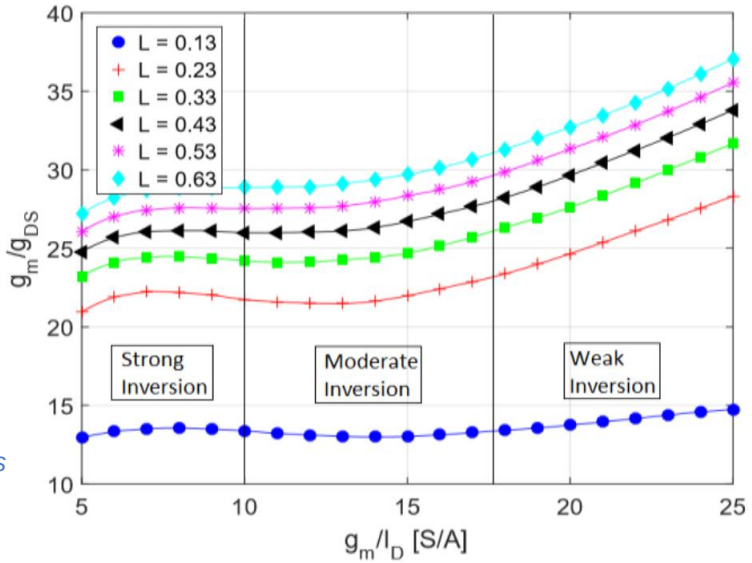
- Black box approach
- Design of Experiments
- Intuitive Design





P. G. A. Jespers and B. Murmann, *Systematic Design of Analog CMOS Circuits Using Pre-Computed Lookup Tables*. Cambridge University Press, 2017.

$$\frac{\eta g_m \phi_t}{I_D} = \frac{2}{1+\sqrt{1+if}} \quad \Rightarrow \quad \frac{g_m}{I_D} = \frac{2}{\eta\phi_t\left(1+\sqrt{1+if}\right)}$$

Circuit Level – Find the best Trade-off

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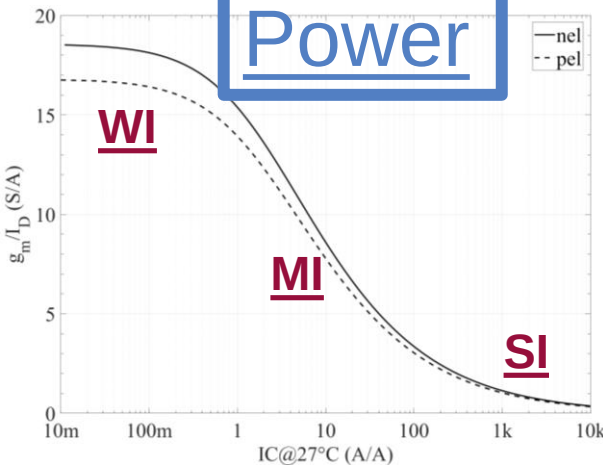
- EDA Optimization problems

Power



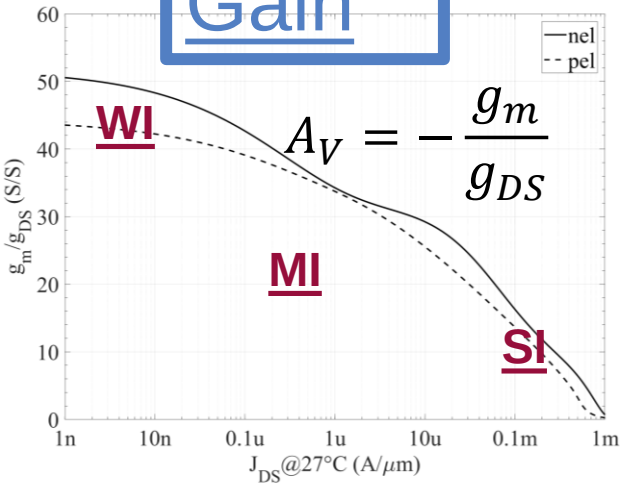
$$P = V_{DD} \cdot \sum I_D$$

$$J_{DS} = \frac{I_D}{W}$$

Area

$$S = L \cdot \sum W_i$$

Gain

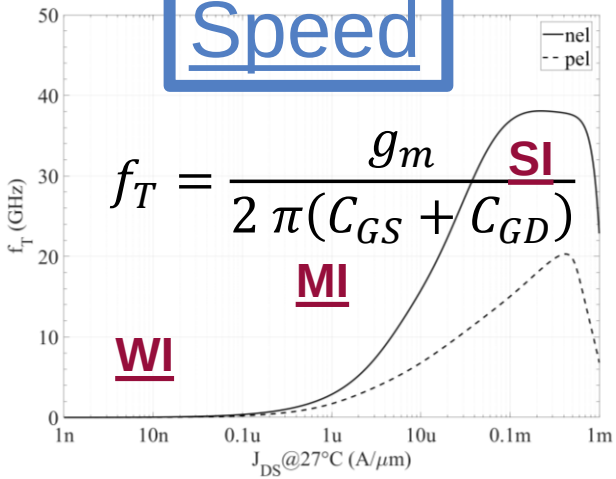


$$A_V = -\frac{g_m}{g_{DS}}$$

Noise

$$f_{CO} = \frac{K_f}{C_{ox}L} \cdot \frac{g_m}{I_D} \cdot \frac{J_{DS}}{4kT\gamma}$$

Speed



$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})}$$

$$\frac{GBW}{SR} = \frac{g_m}{I_D}$$

J. Ou and P. M. Ferreira, "Implications of Small Geometry Effects on gm/ID Based Design Methodology for Analog Circuits," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 1, pp. 81–85, Jan. 2019.
J. Ou and P. M. Ferreira, "A gm/ID-Based Noise Optimization for CMOS Folded-Cascode," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 61, no. 10, pp. 783–787, Oct. 2014.

System Level – Hybrid ADCs

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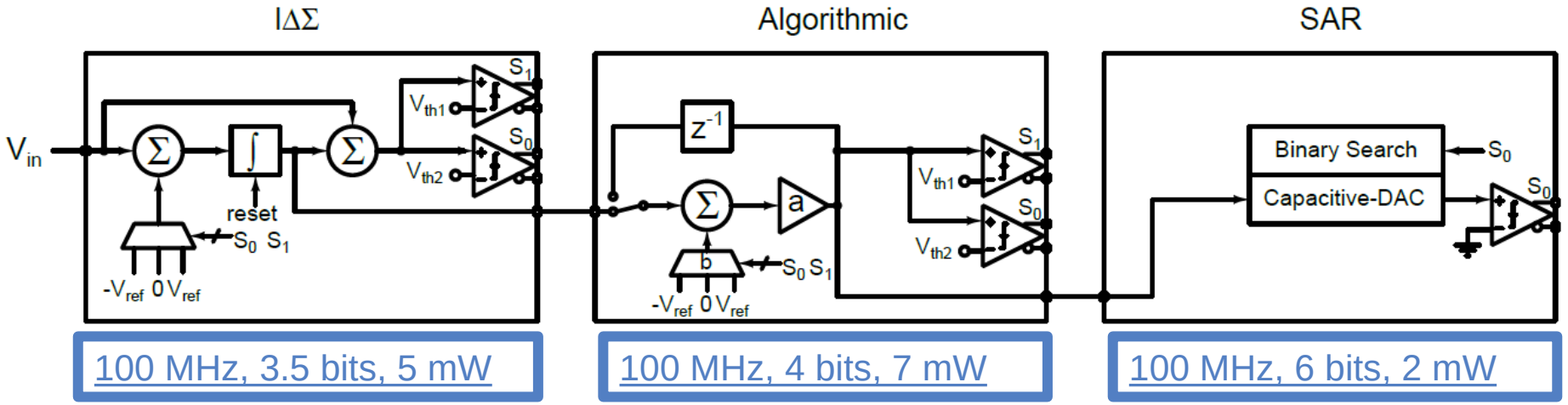
- Novel Topologies as hybrid and heterogeneous solutions
- Performance constraint share
  - Faster, higher resolution and low power



Ph.D. L. Cron ADC proposal

A. V. Fonseca, et al. "A Temperature-Aware Analysis of SAR ADCs for Smart Vehicle Applications," *J. Integr. Circuits Syst.*, vol. 13, no. 1, pp. 1–10, Aug. 2018.

System Level – MEMS instrumentation

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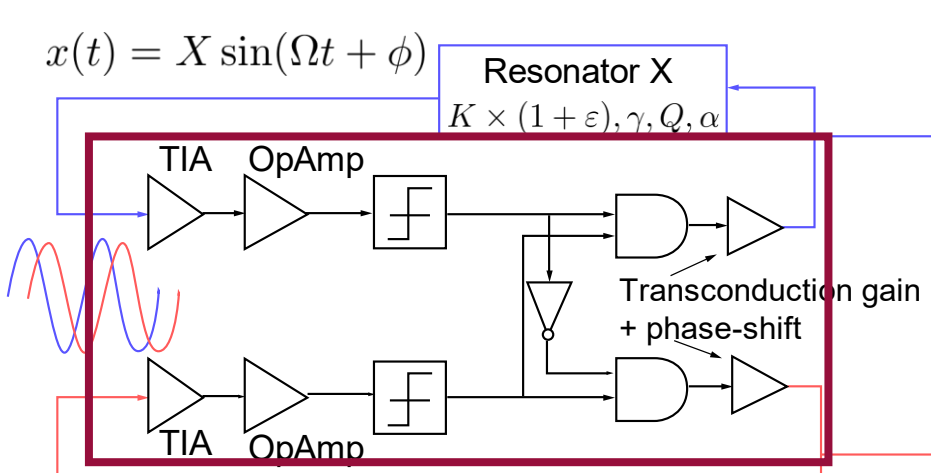
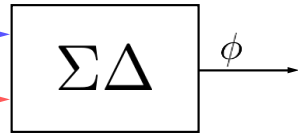
Mechanical
(M. Gouspy)

Electronics
(João R. R. O. Martins)



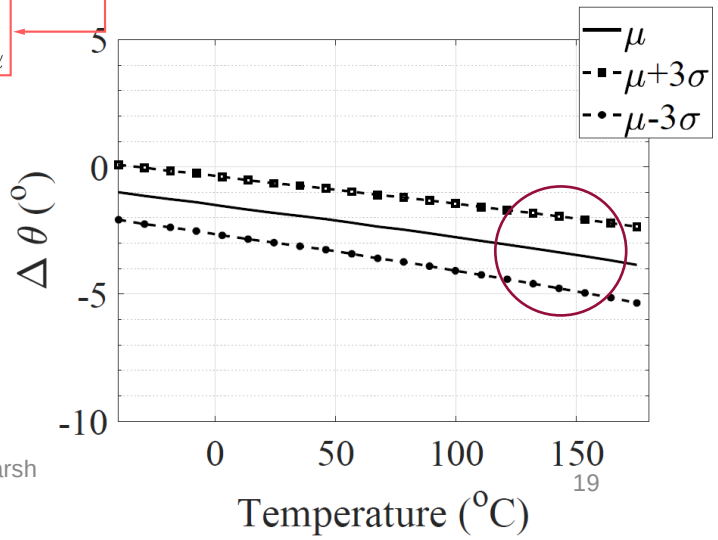
Converter
(A. Mostafa)



$$\phi = \frac{\pi}{2}\cdot(1+2Q\varepsilon)$$

Unreliable Electronics

$$\phi = \frac{\pi}{2}\cdot\left(1+2Q\left(\varepsilon+\frac{\sqrt{2}}{2Q}\cdot\Delta\theta\right)\right)$$



P. M. Ferreira, et al, "Process-Voltage-Temperature Analysis of a CMOS-MEMS Readout Architecture," in *Proc. IEEE Design, Test, Integration & Packaging of MEMS/MOEMS*, 2019, pp. 1–4.

Content

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More than Moore: Silicon in Photonics

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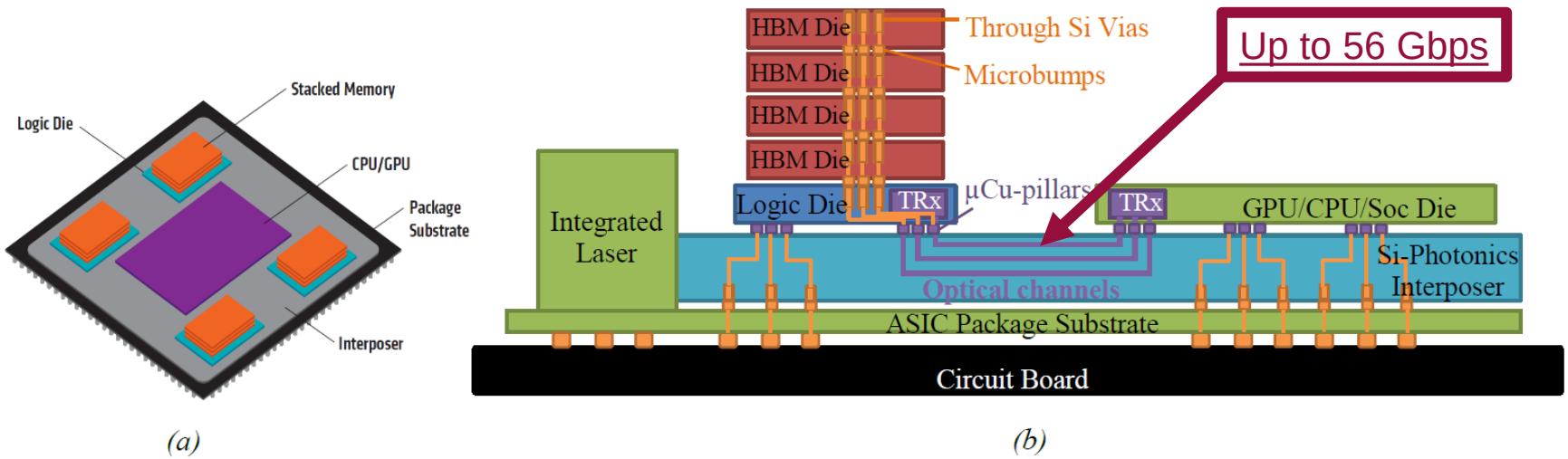

- Better data transmission – Light is not bounded to wire connection limitations (8 Gbps for PCIe)
- Higher integration costs – Requires a SiP post processing
- Smaller footprint – Computer Motherboard in a single ASIC

A 0.9 pJ/bit, low-ER SiP transmitter

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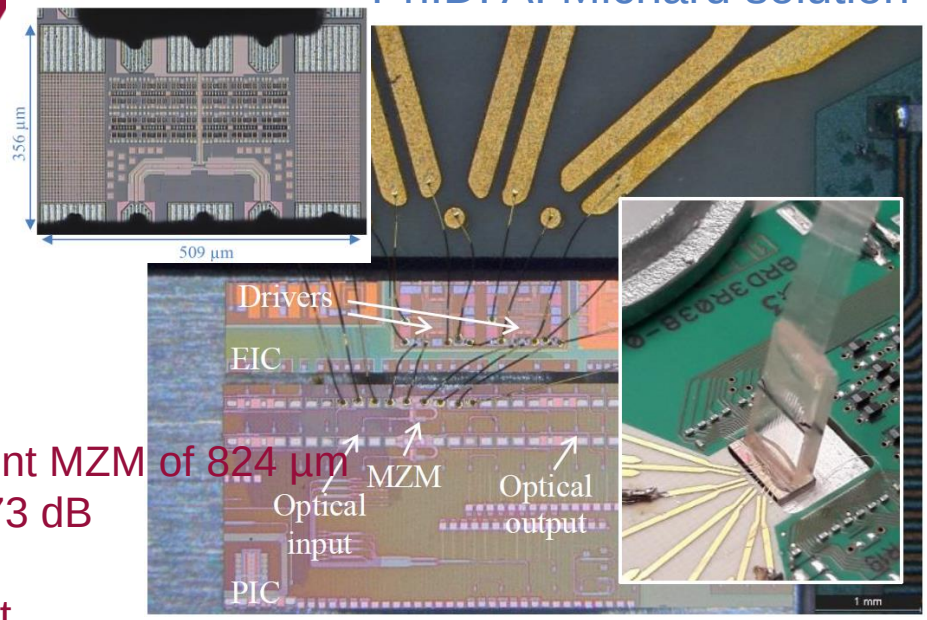
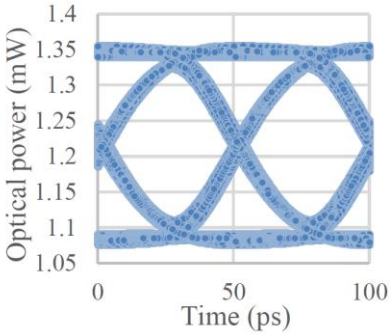
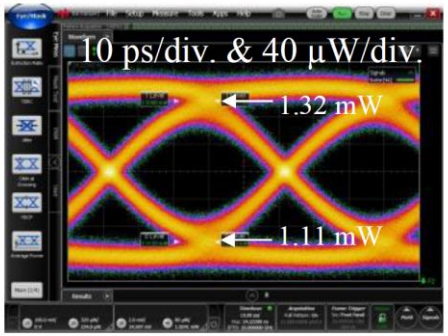
Ph.D. A. Michard solution



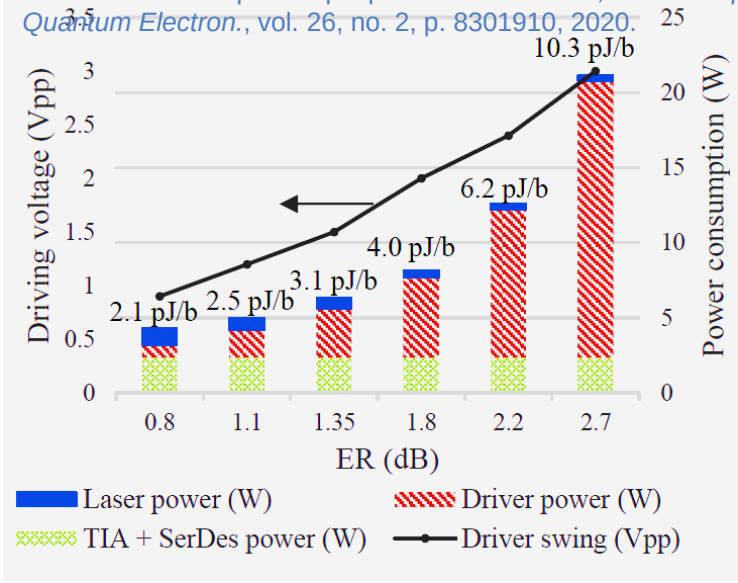
1 segment MZM of 824 µm
ER = 0.73 dB
20 Gbps
0.9 pJ/bit





- Heterogenous SiP solution – bond wires connection
- System-level Optimization
  - Power consumption
  - Extinction Ratio reduction
  - 20 Gbps data rate

A. Michard, et al., "A sub-pJ/bit, low-ER Mach-Zehnder-based Transmitter for chip-to-chip Optical Interconnects," *J. Sel. Top. Quantum Electron.*, vol. 26, no. 2, p. 8301910, 2020.



More than Moore: Artificial Intelligence

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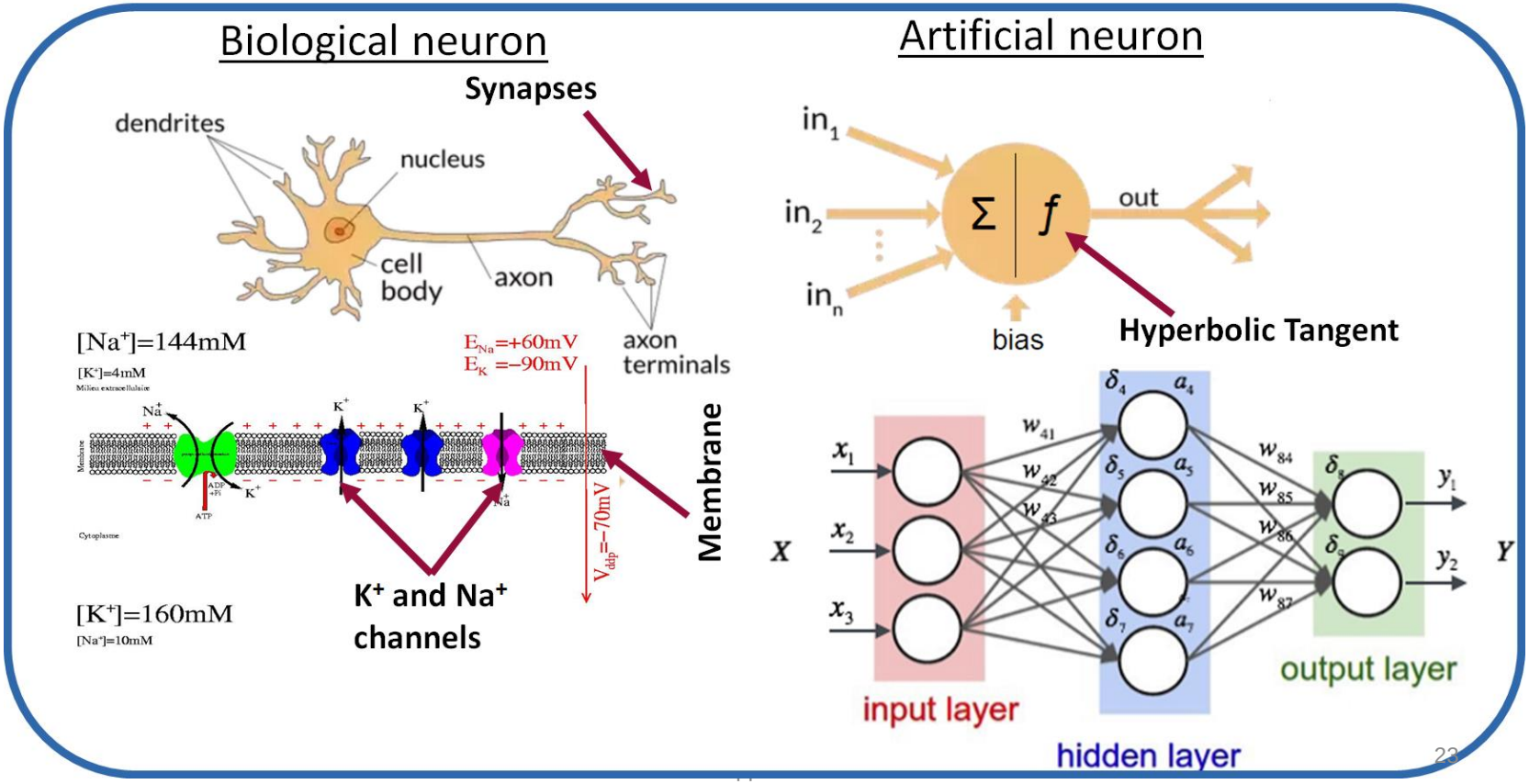
- Biological Solutions
  - Ion charge conduction
  - Living cells
- Software Solutions
  - Binary based
  - Von Neumann Computer



Neuromorphic Analog Spiking-Modulator

a 55 nm Integrated SNN solution

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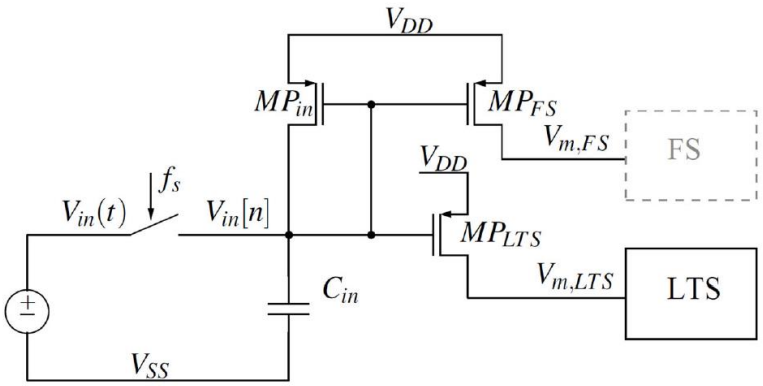
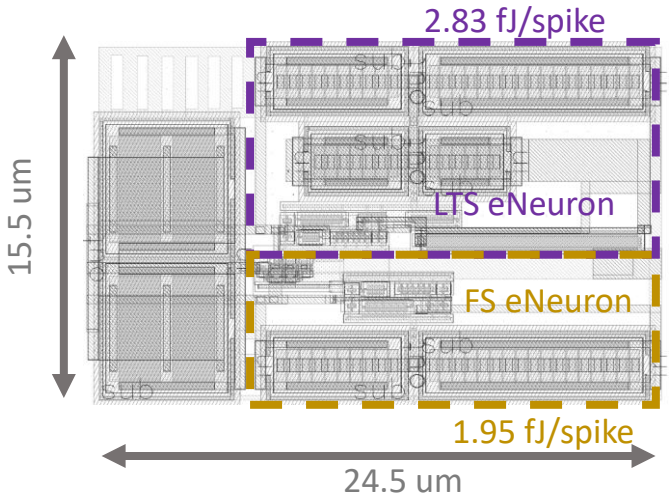
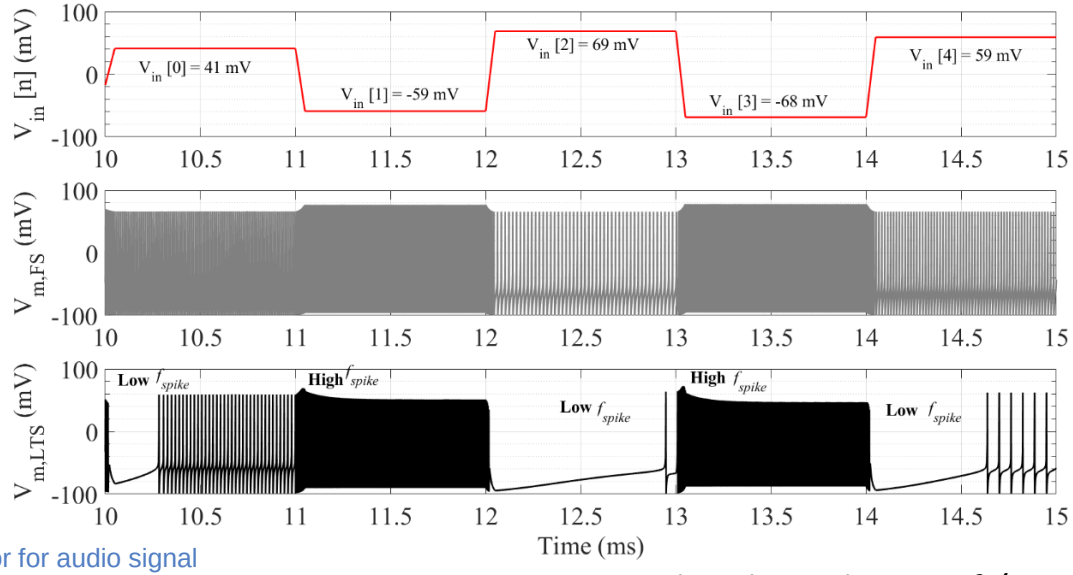


- Analog Hardware Solutions
  - Neuron model validated

    I. Sourikopoulos *et al.*, "A 4-fJ/spike artificial neuron in 65 nm CMOS technology," *Front. Neurosci.*, vol. 11, no. 123, pp. 1–14, Mar. 2017.
  - Lack of plasticity in synapses

    G. Indiveri *et al.*, "Neuromorphic silicon neuron circuits," *Front. Neurosci.*, vol. 5, no.5, pp. 1–23, May 2011.





Ferreira, P.M., *et al.* Neuromorphic analog spiking-modulator for audio signal processing. *Analog Integr Circ Sig Process* **106,** 261–276 (2021). https://doi.org/10.1007/s10470-020-01729-3

NASP: 9 bits de resolution, 8 fJ/conv

Content

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- Why do we need Research in Electronics ?
- How do we do Research in Electronics ?
- Trend Research
  - More than Moore Analog Electronics
  - Electronics for Harsh Environments

Harsh Environments: Radiation and Aging

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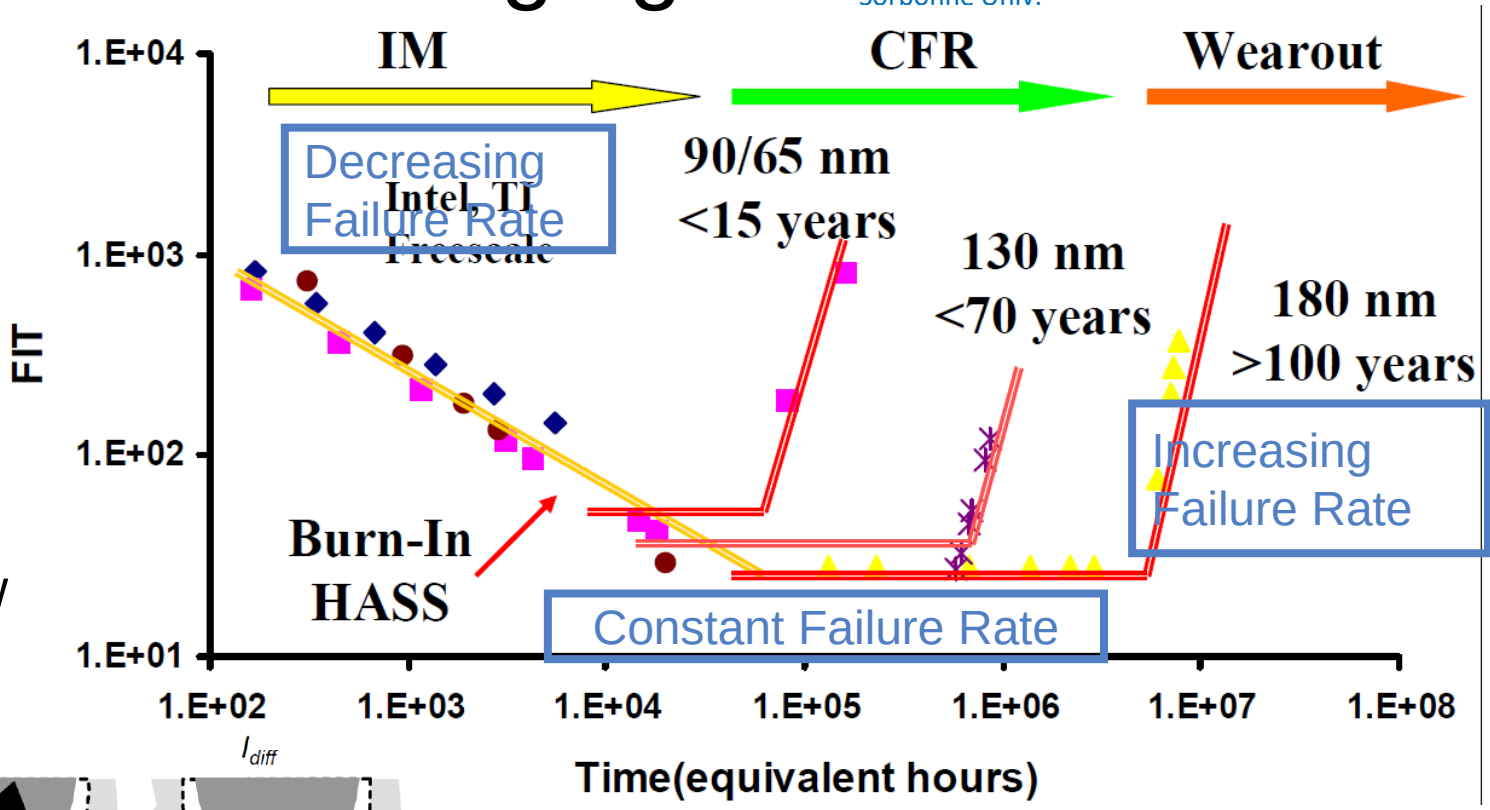
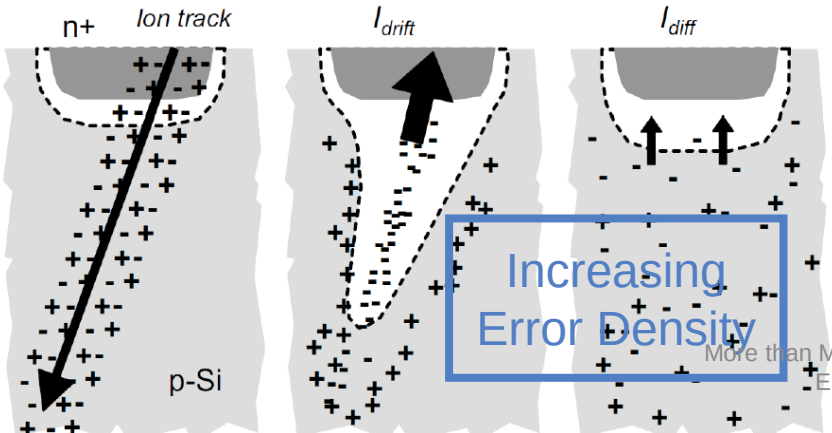
- Failure is increasing in nanometric electronics
- Transistor lifetime below few years!





M. White and Y. Chen, "Scaled CMOS Technology Reliability Users Guide," JPL Publication 08-14 3/08, 2008. (NASA report)

Transistor-level: Reliability Resilience

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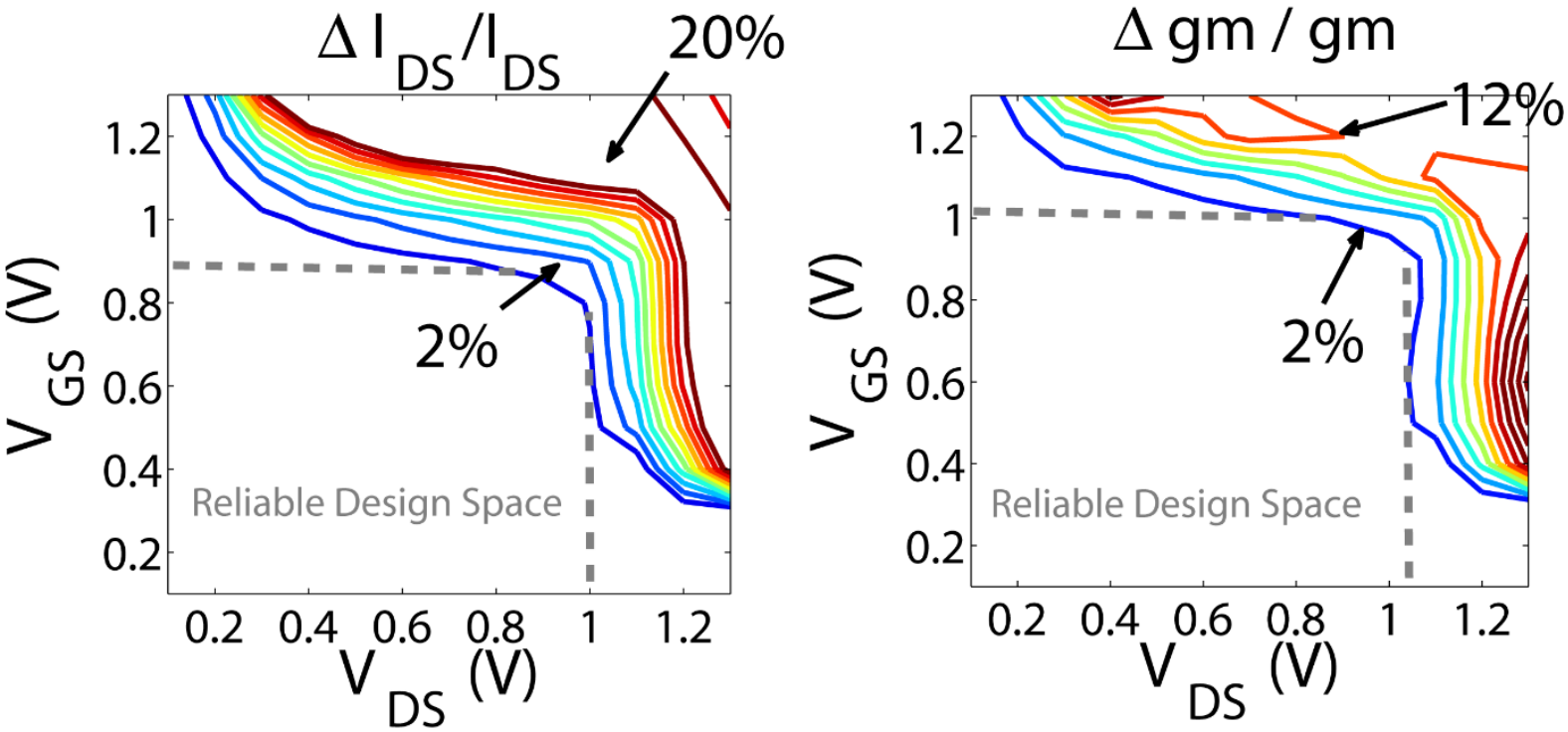

- Modeling HCI and NBTI of ST 65 nm
- Enable a g_m/I_D methodology
- Negligible aging – reliable design space

P. M. Ferreira, H. Petit, and J.-F. Naviner, "A New Synthesis Methodology for Reliable RF front-end Design," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2011, pp. 1–4.
P. M. Ferreira, H. Petit, and J.-F. Naviner, "A synthesis methodology for AMS/RF circuit reliability: Application to a DCO design," Microelectron. Rel., vol. 51, no. 4, pp. 765–772, Dec. 2010.

System-Level: Faulty building blocks

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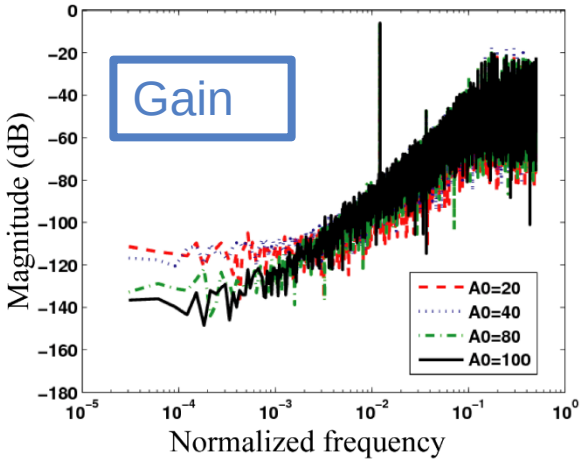
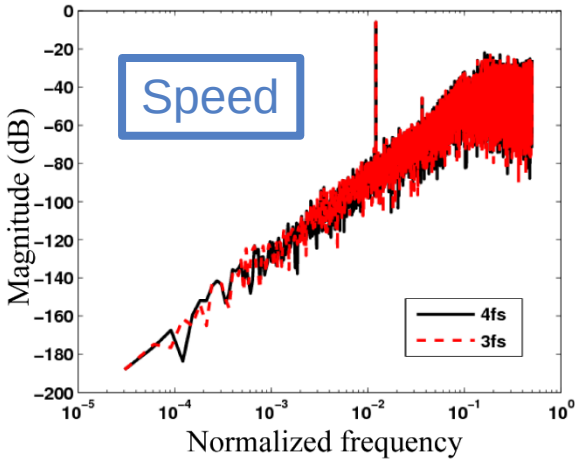
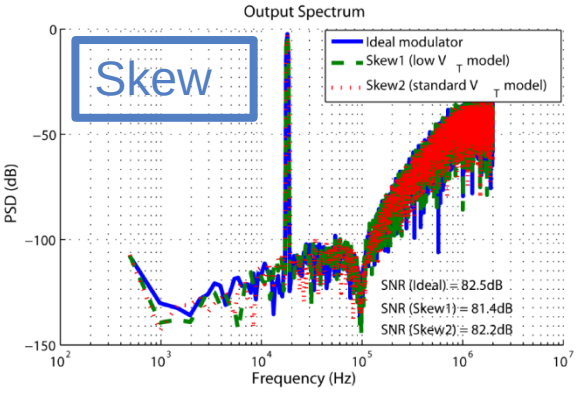
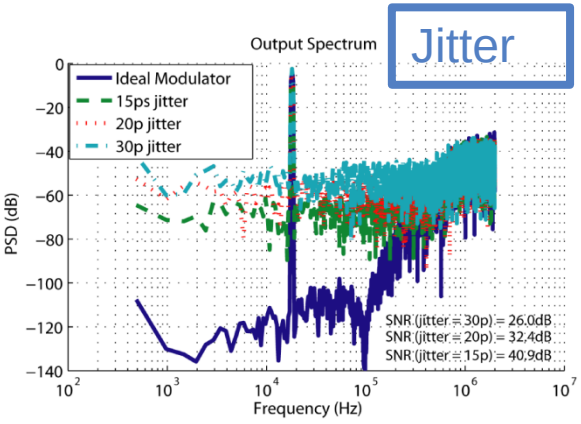
- Continuous Time ΣΔ ADC
- Building block failure tests

- OpAmp Failure
  - Gain drop
  - GBW limitation
- Clock
  - Skew
  - Jitter









P. M. Ferreira, H. Cai, and L. Naviner, "Reliability Aware AMS / RF Performance Optimization," in *Performance Optimization Techniques in Analog, Mixed-Signal, and Radio-Frequency Circuit Design*, Eds. IGI-Global, 2014, pp. 28–54.

Harsh Environments: High Temperature

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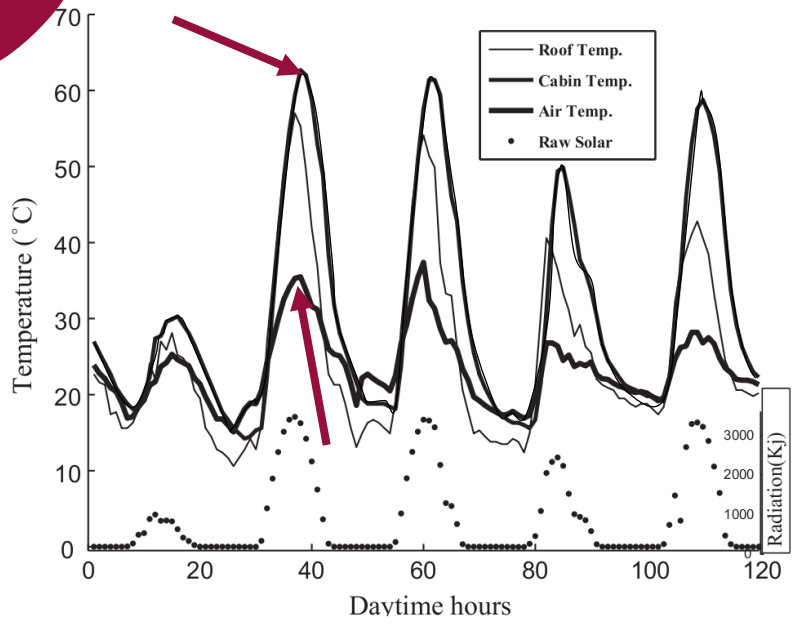

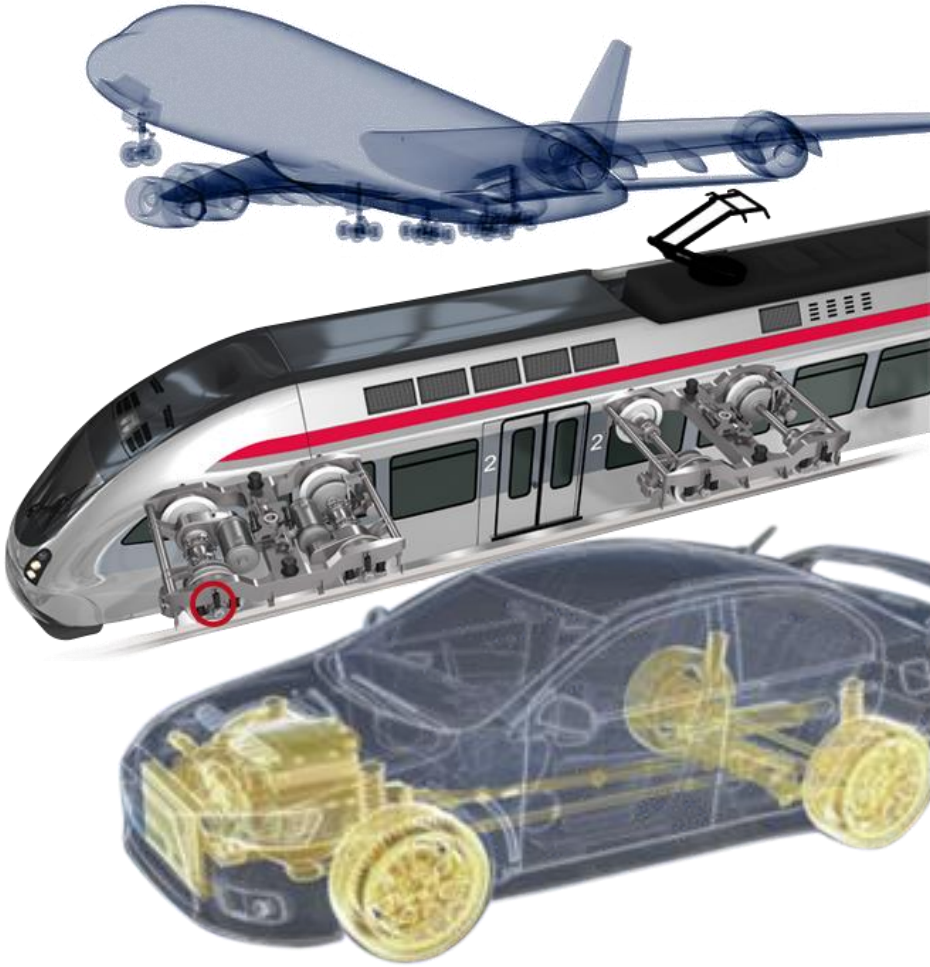

- Smart Vehicles – efficiently sense and communicate with other nearby devices
- Safety in working environment – high temperature
- Low costs – use standard processes, digital-enabled

More than 200 sensors expected

Harsh Environments: High Temperature

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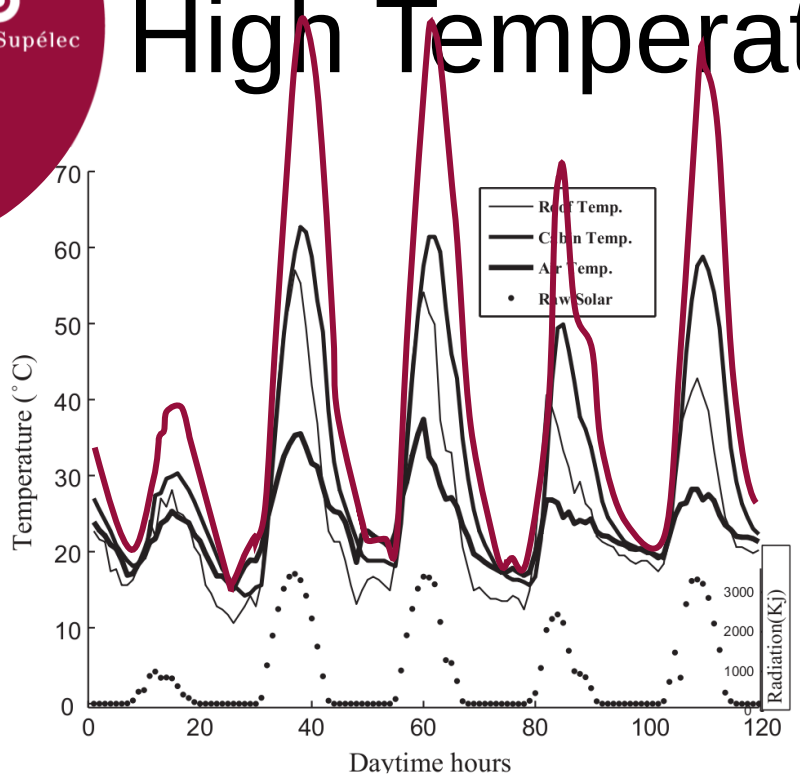

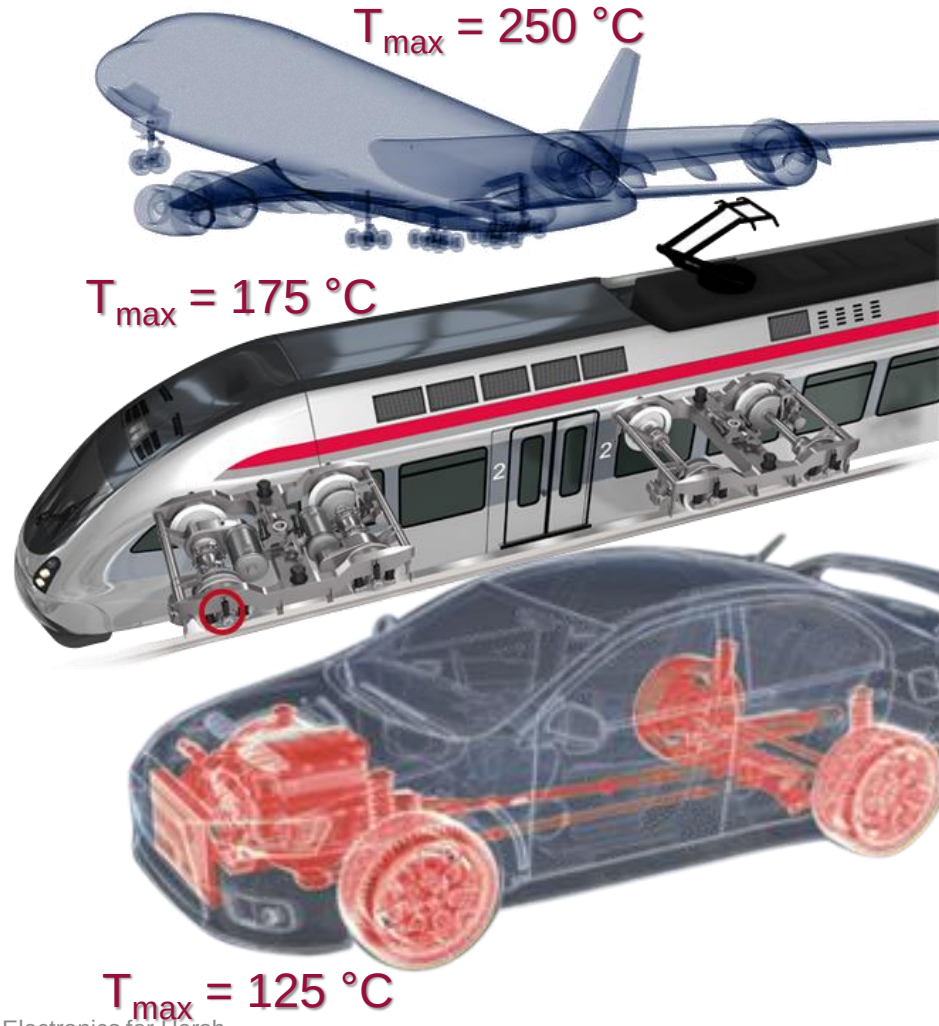

- Smart Vehicles – efficiently sense and communicate with other nearby devices
- Safety in working environment – high temperature
- Low costs – use standard processes, digital-enabled

g_m/I_D Methodology fails in high temperature

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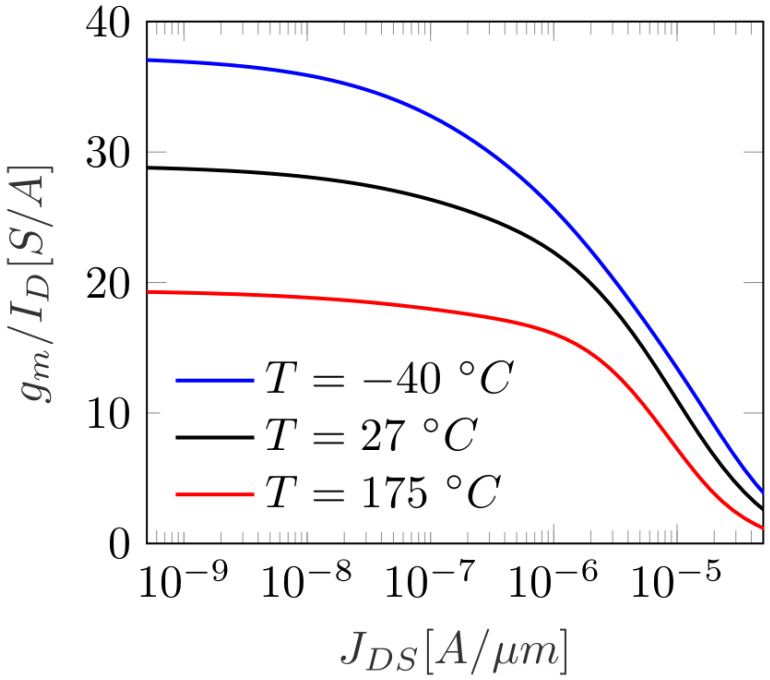

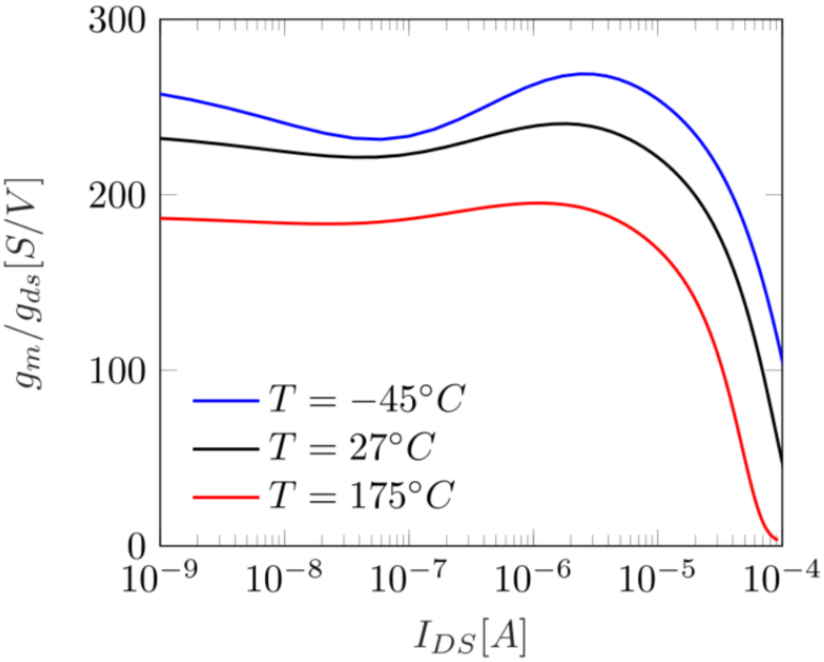

$$\frac{g_m}{I_D} = \frac{1}{\phi_t} \frac{2}{\eta(V_G)(q_{is}(V_G, V_s) + q_{id}(V_G, V_s) + 2)}$$

Temperature Dependency

Temperature Aware g_m/I_D Methodology

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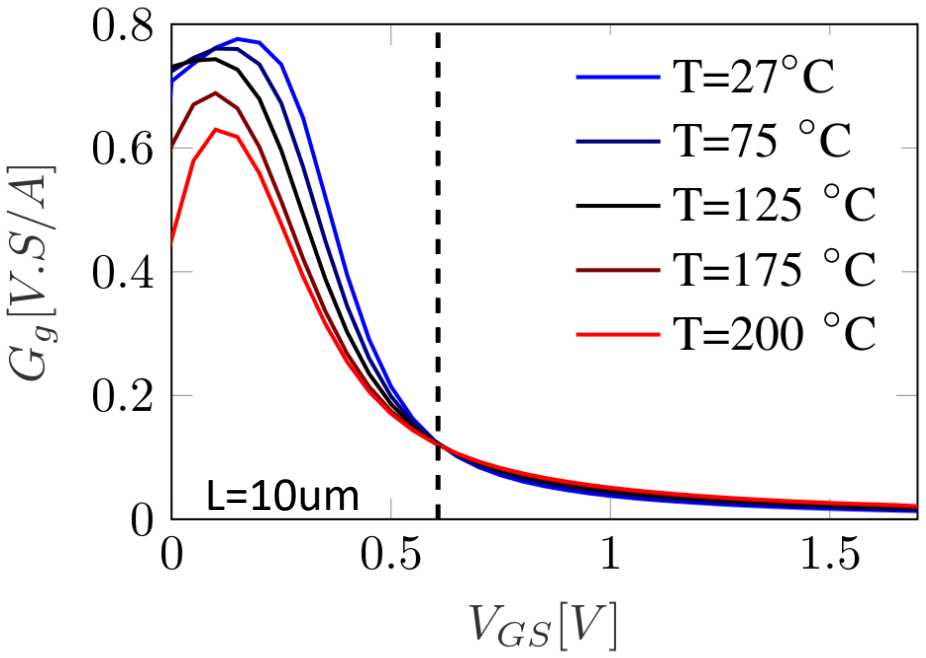
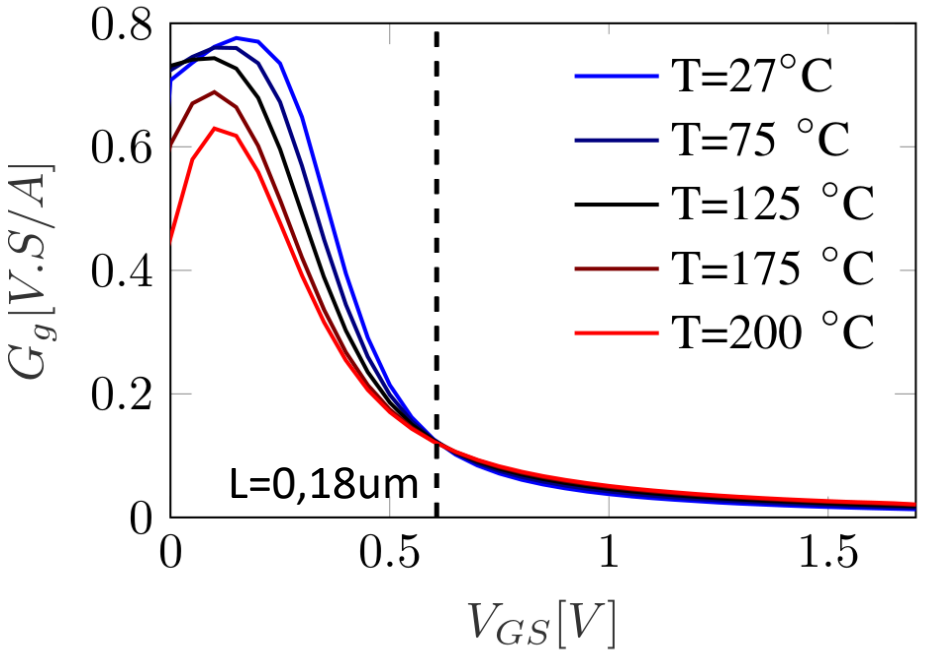
J. R. R. O. Martins, Ph.D. cand methodology





$$\frac{g_m}{I_D} = \frac{1}{\phi_t} G_g$$

Temperature Normalized Parameter

J. R. R. De Oliveira Martins, et al., "A Temperature-Aware Framework on gm/ID-Based Methodology Using 180 nm SOI From −40 °C to 200 °C," in IEEE Open Journal of Circuits and Systems, vol. 2, pp. 311-322, 2021, doi: 10.1109/OJCAS.2021.3067377.

Temperature Aware OTA

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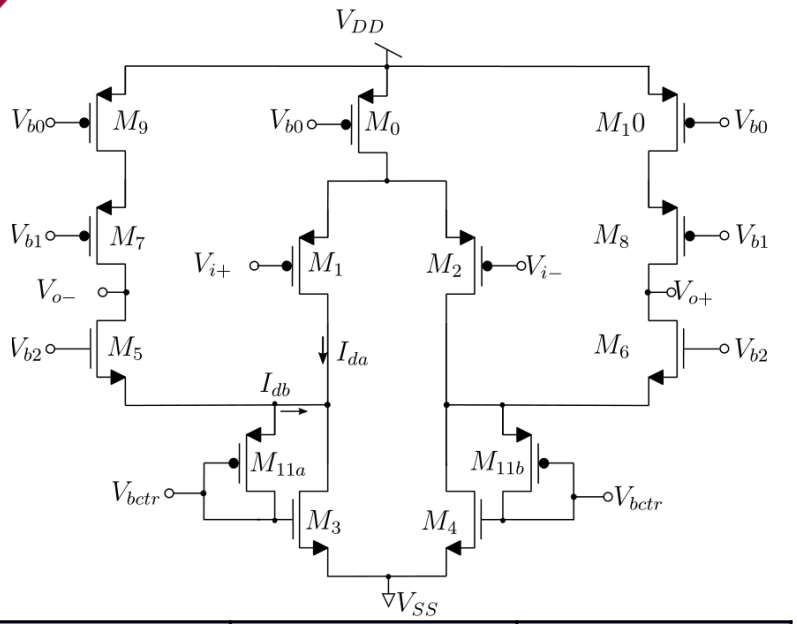
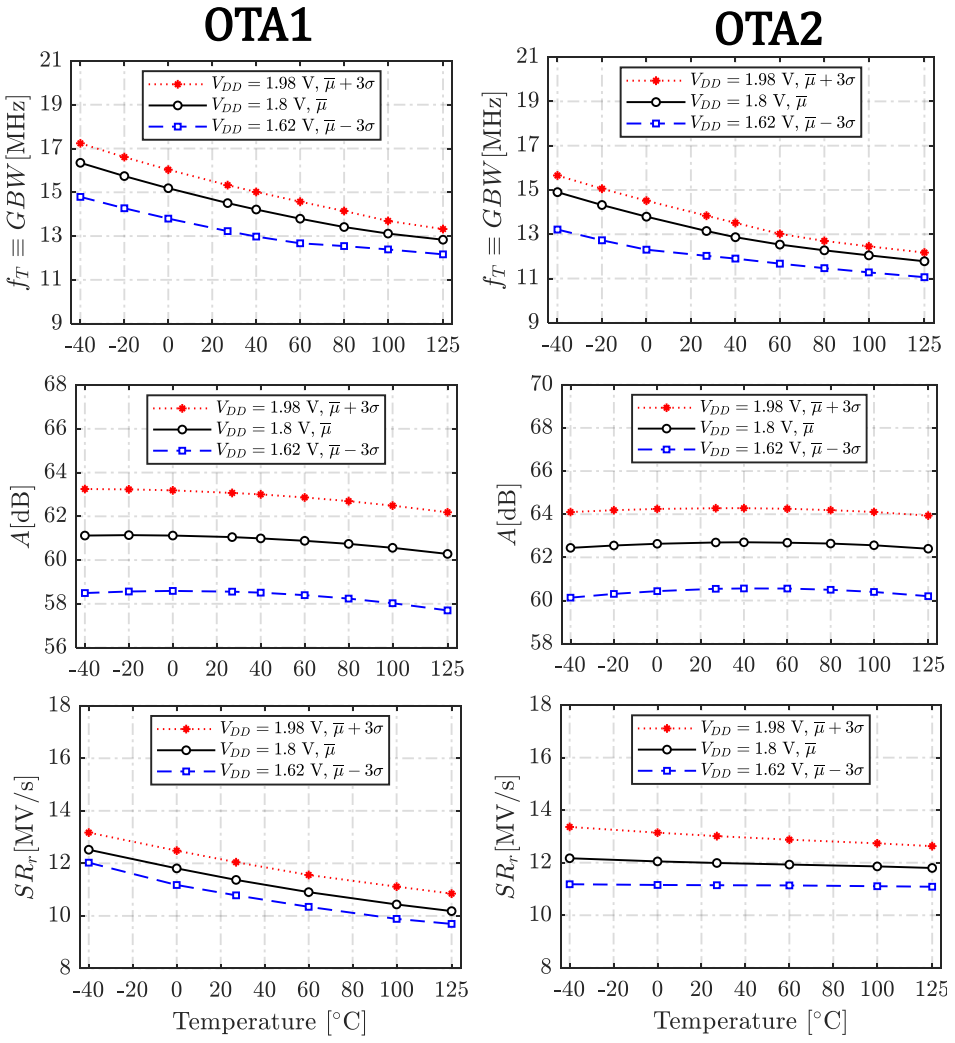
Ph.D. A. Mostafa design



Device	g_m/I_d	To minimize
M_0	6	$S^T_{I_{DS}}$
$M_{1(2)}$	9	$S^T_{g_m}$
$M_{3(4)}$ and $M_{5(6)}$	5 ($L = 3\mu m$)	$S^T_{I_{DS}}$ and $S^T_{g_{ds}}$
$M_{7(8)}$ and $M_{9(10)}$	6 ($L = 3\mu m$)	$S^T_{I_{DS}}$ and $S^T_{g_{ds}}$



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Thank you very much

Questions?

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