Open Software for Open Hardware and the Licenses

Vers une licence libre pour les circuits intégrés sur silicium

LIP6, Sorbonne Université - CNRS
Equipe CIAN : FOSS EDA for analog and mixed circuit design

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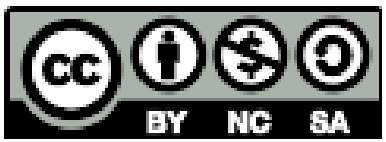


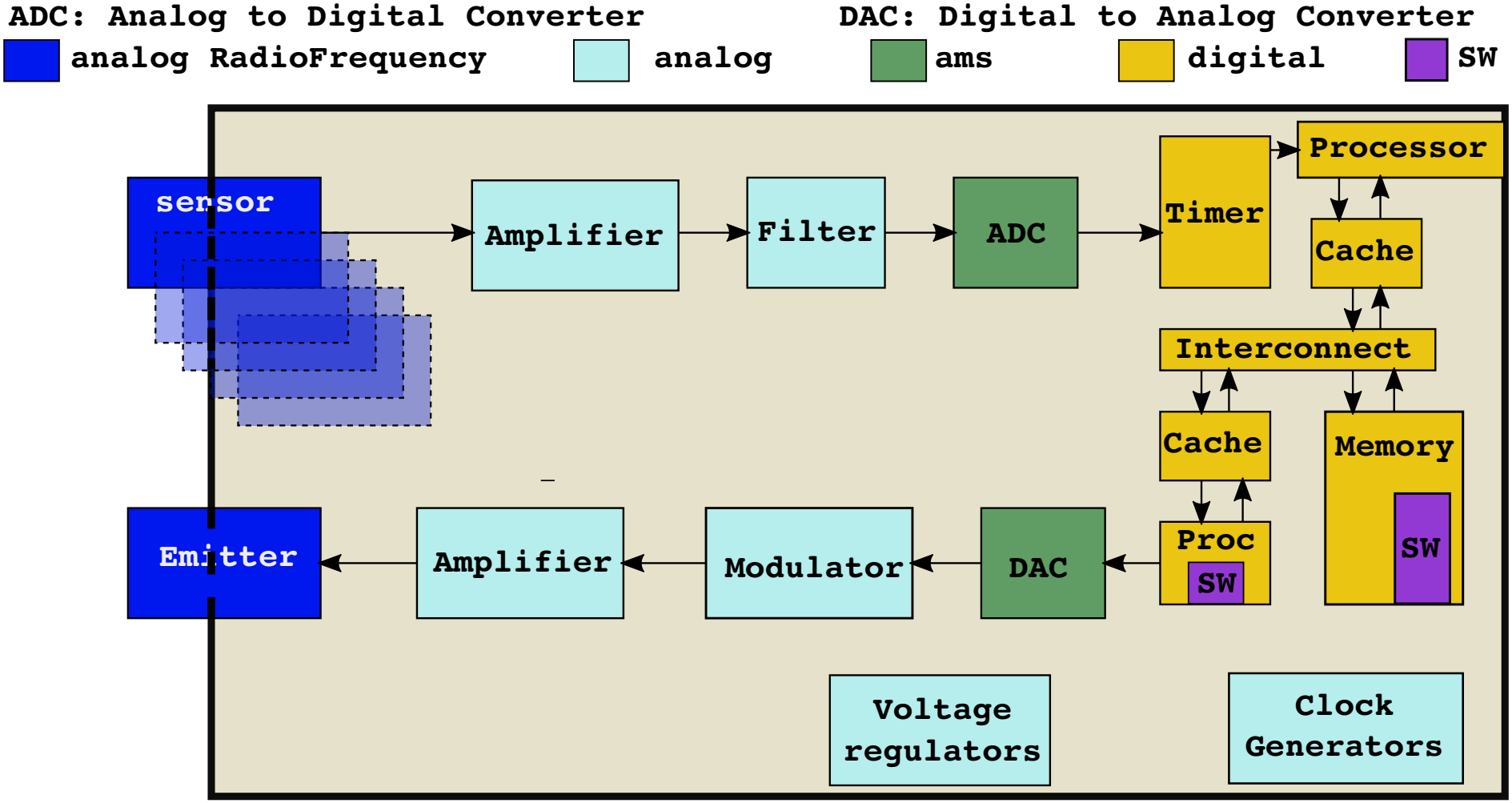
Forewords


soo dhawaw
pô la bwam
benvenuti
Добре Дошол
又欠迎
yôkoso
Karibu
willkòmmen
bon bini
awaa waa atuu
fáitre
Καλώς ήλθατε
BIENVENUE
welkomma
Welcome
bem-vindo
välkommer
tervetuloa
خوش آمدید
bel bonjour
üdvözlet
vaelkomin
tere tulemast
chàa mòng
benvido
degemer mad
ani Kié
binlavnu
namaste
bonavinuta
Kakwaɔ
welkum
benvinguts

Plan

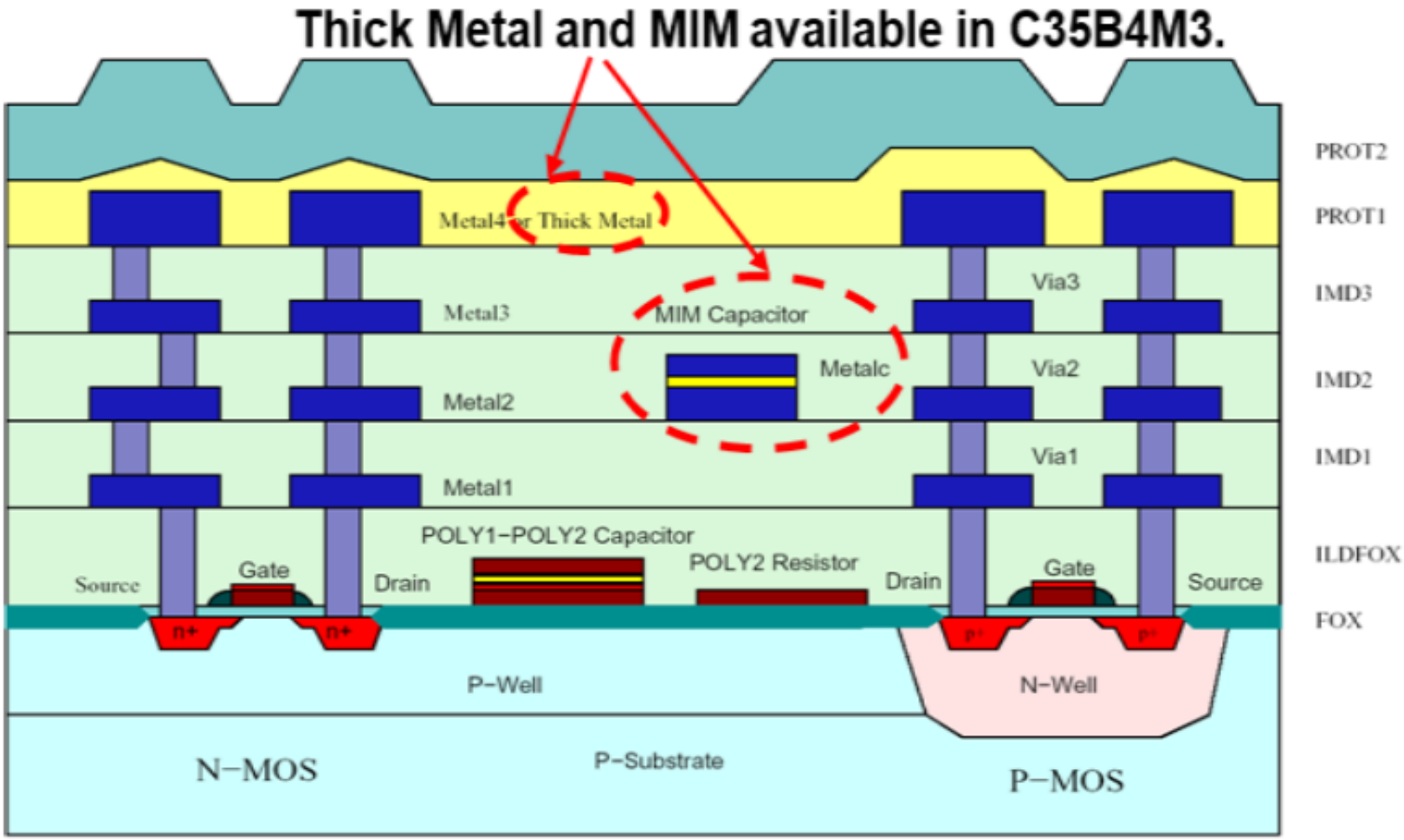
Plan

Introduction : Application On Chip (on Silicon)



Analog and Mixed Signal (ams) System

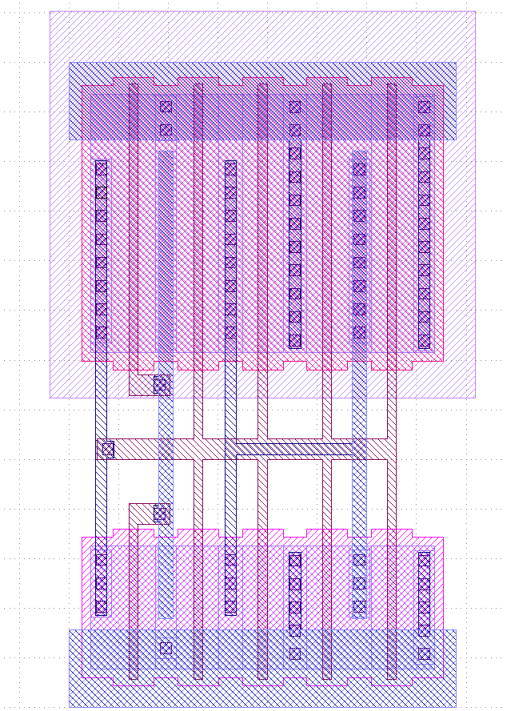
CMOS Integration



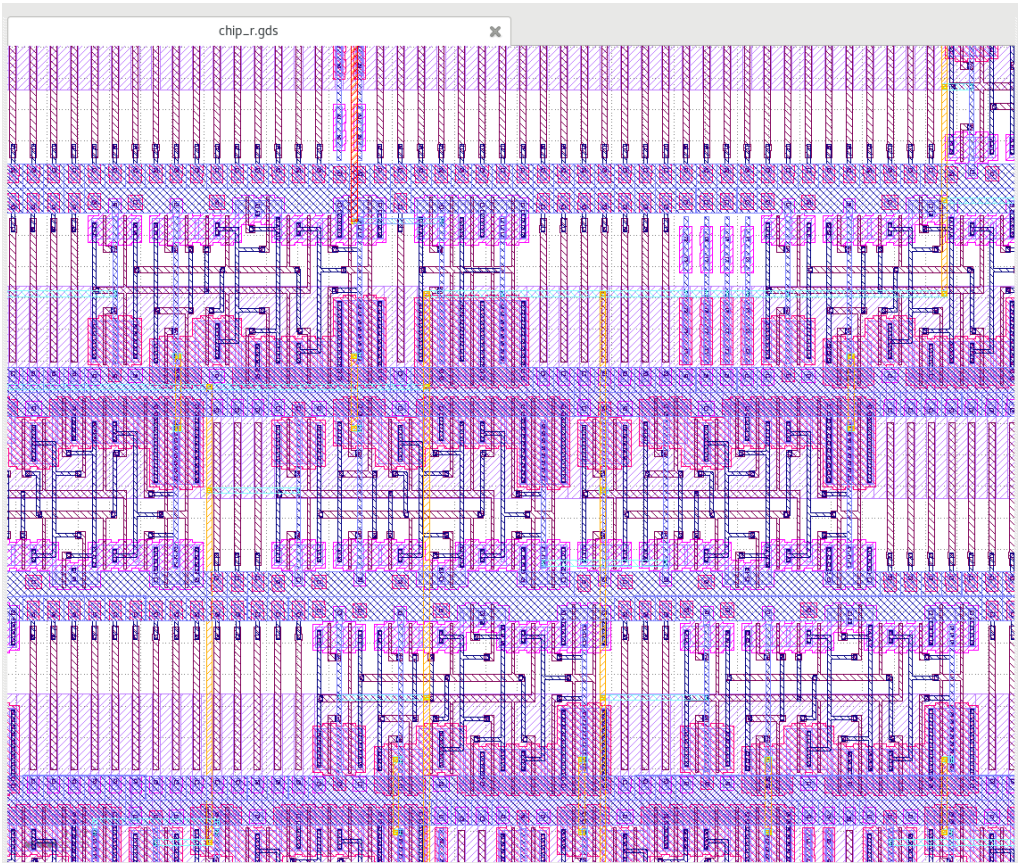
CMOS technology, vertical cross section of a chip [1]
3D layers, each layer height is specific to a process

1. https://mycmp.fr/wp-content/uploads/2021/03/4_matureprocesses_lk.pdf

Description sent to the Foundry

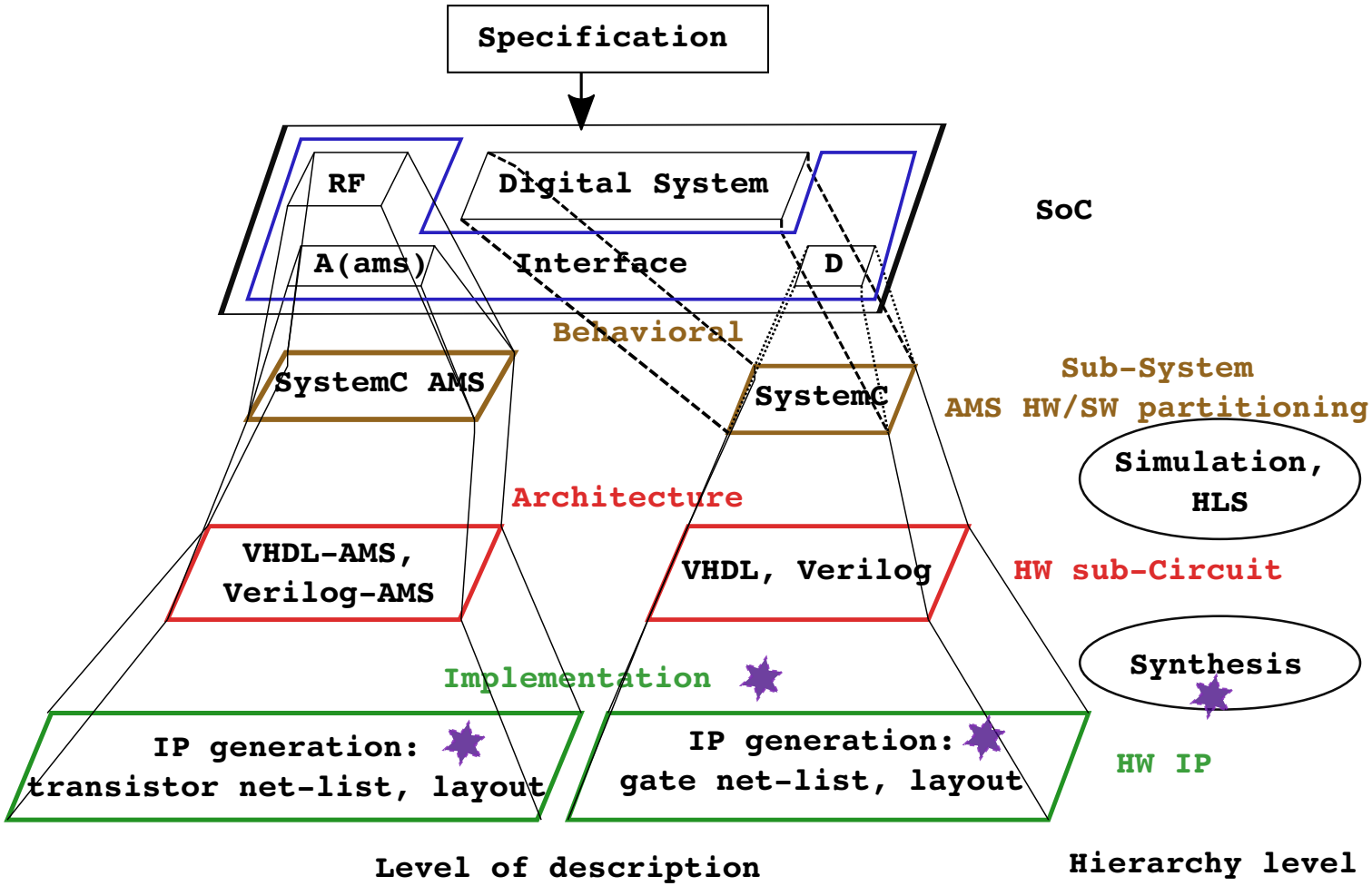


Standard Cell : Buffer
Top view : 2D sizes
specific to a Library
one color = one layer



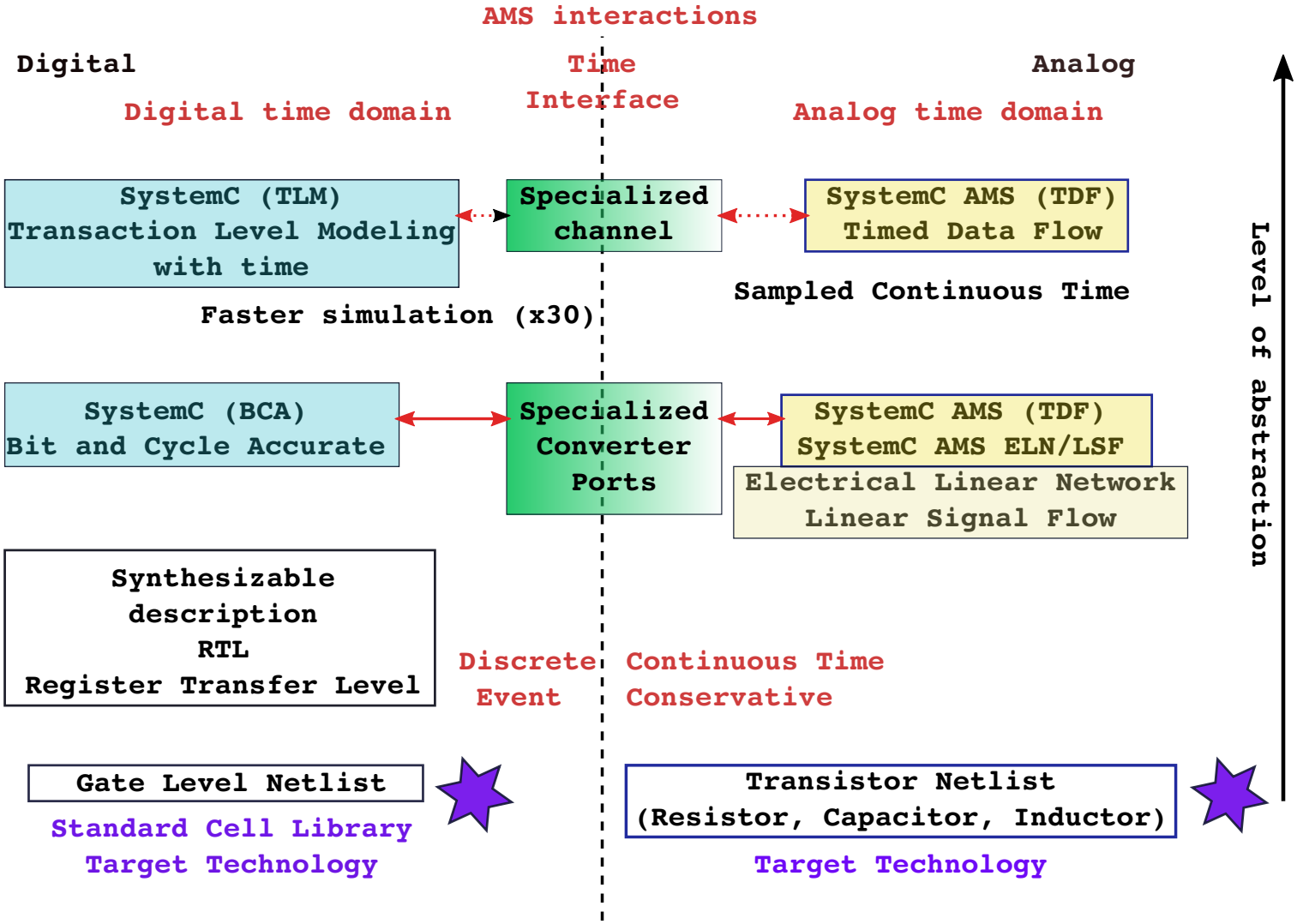
Chip Layout : 2D representation of layers
Top view after Placement and Routing
(over the cells) of standard cells

Design Flow for Heterogeneous (AMS-HW + SW) system



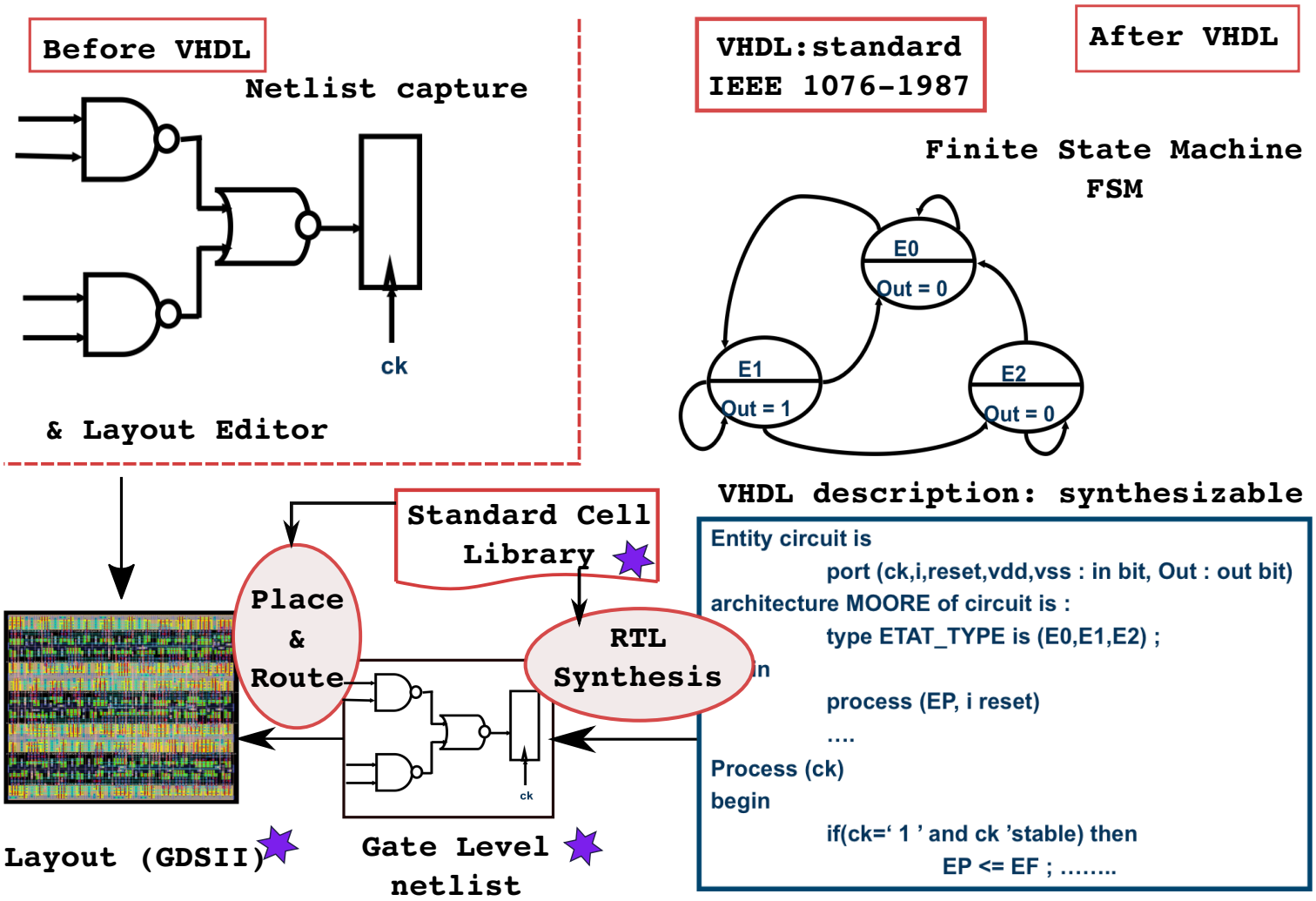
Analog and Mixed Signal (ams) System Design
showing target technology stepping into play (purple stars)

Simulation of Heterogeneous (AMS-HW + SW) system



Models : Level of Abstraction, and simulation speed tradeoff showing target technology stepping into play (purple stars)

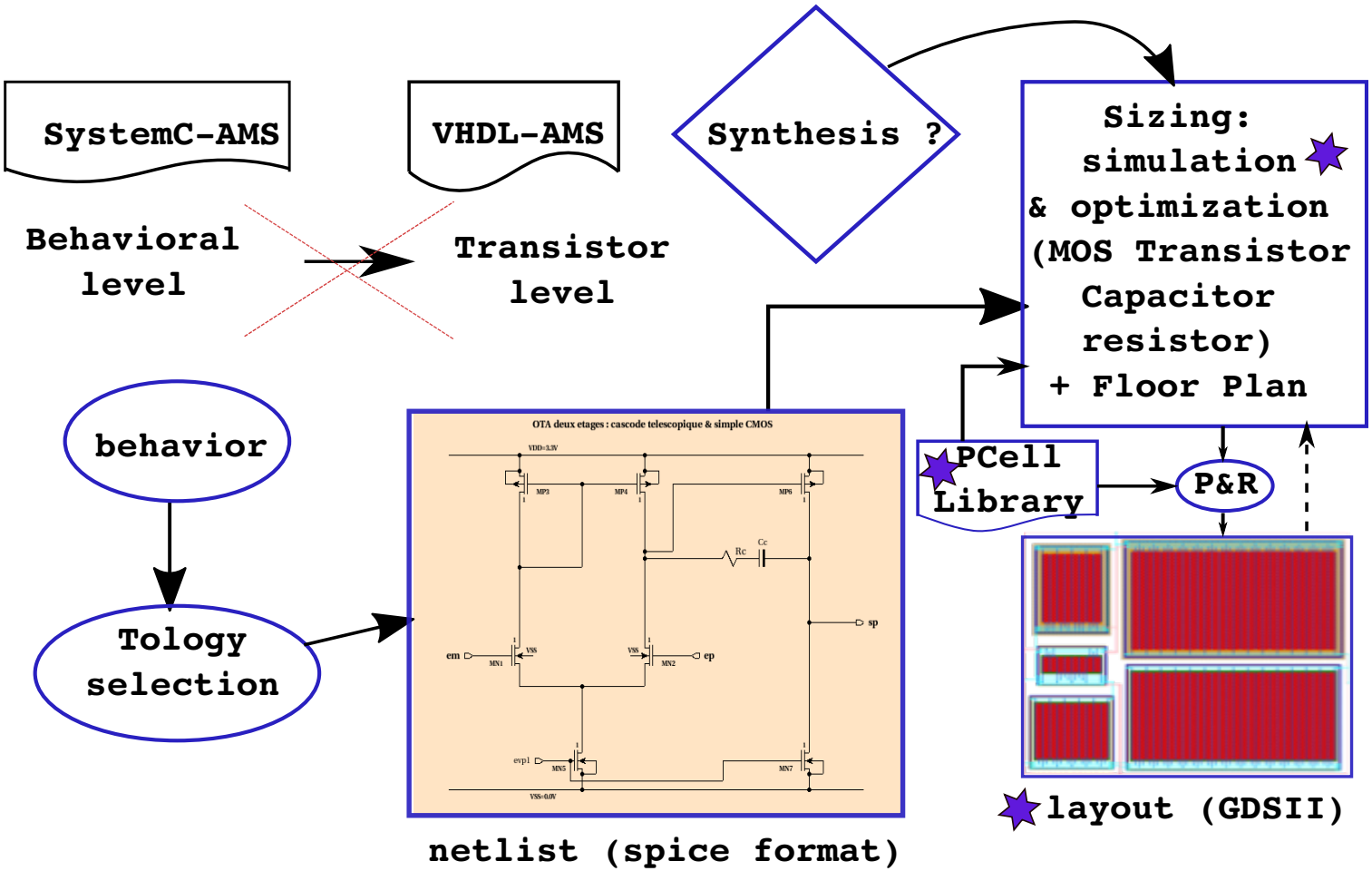
Design Flow for HW digital IP



Digital IP Design

with technology data coming into play (purple stars)

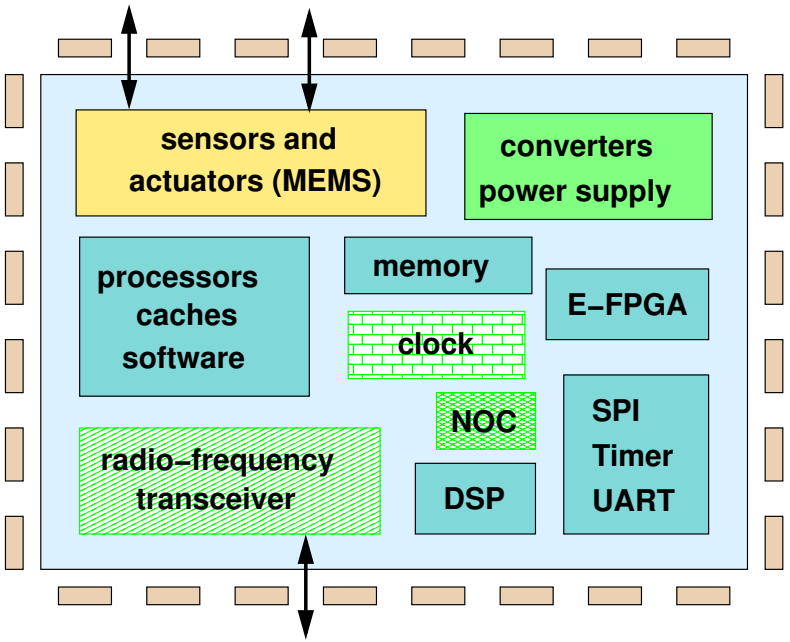
Design Flow for HW analog IP



Analog IP Design

showing target technology key role (purple stars)

Designing the On Chip Application : Costs and Constraints



AMS SoC in CMOS

- SW Tools' licenses cost is prohibitive for SMEs, and Universities
- Circuit fabrication is costly, though **Multi Project Wafer**
- No sharing of IP due to foundry Non Disclosure Agreement (**NDA**)
- Non modifiable EDA-SW limit integration of specific algorithms
- HW IP perf. cannot be enhanced
- NO replication of experiments
- Prevents the creation of a community

NOC : Network On Chip
DSP : Digital Signal Processor
e-FPGA : embedded Field-Programmable Gate Array
SPI : serial Peripheral Interface
UART : Universal Asynchronous Receiver Transmitter

When *proprietary* technology processes are involved : PDK

- Standard Cell library (Digital)
  - Gate level Simulation and Logical Synthesis (Timing Characterization)
  - Layout
- Parameterized Cells (MOS transistor, Resistor, Capacitor, Inductors)
  - Transistor Level Simulation and Sizing (Biasing, Transient analysis, Noise analysis)
    - ⋆ MOS transistor model (Berkeley BSIM3v3 MOS, Berkeley BSIM4 MOS, NXP PSP MOS, EPFL EKV, cea FDSOI...)
  - Layout

Process Design Kit PDK (subject to authorization - NDA contract)

Libraries (Standard Cells, Parametrized Cell, Input Ouput Cells)
Design Rule Manual (DRM) : manufacturing rules for layout
Parameter files for EDA tools (simulation, synthesis, place&route, Design Rule Check (DRC), Electrical Rule Check (ERC), Design for Yield, Matching, Parasitic Extraction, Timing Analysis,...)

When Data Exchange Formats and Standards are involved

- Simulation and synthesis : a hierarchy of cells
  - SystemC (IEEE) 1666-2005, 2011, SystemC AMS extensions 1666.1-2016
  - Gate level, RTL digital : VHDL (IEEE 1076-1987, 1076-1993, 1076-2008), Verilog (from Cadence to IEEE 1364)
  - Berkeley Logic Interchange Format (BLIF) : a logic-level hierarchical circuit in textual form
  - Liberty Timing Files (LIB). ASCII + timing characterization of standard cells (Synopsys) https ://news.synopsys.com/index.php ?item=123415
  - Transistor level simulation (Spice 1970, ISO 15504 IEEE milestone). L. Nagel was awarded the 2019 IEEE Donald O. Pederson Award in Solid-State Circuits for the development of SPICE.
- Circuit Layout : Place&Route a hierarchy of cells
  - Library Exchange Format (LEF) from Cadence
  - Design Exchange Format (DEF) from Cadence
  - GDSII. De facto industry standard for data exchange of integrated circuit or IC layout artwork. It is a binary file format representing planar geometric shapes, text labels, and other information about the layout in hierarchical form.

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Free and Open Source SW and Open HW History

- Electronic Design Automation (EDA) FOSS
  - Part of the Free Open Source Movement (Linux, GPL) [2]
  - Free Open Source Software (FOSS) : freedom to run, copy, share, study, modify and improve the software
  - Univ. Berkeley pioneer with the circuit simulator Spice
  - Mostly digital [3] : Alliance, QFLOW, Yosys, SpinalHDL, ...

- Open Source Hardware (OHW) context
  - Technology-Based extension of Do-it yourself movement (DIY)
  - Extending the Worldwide Makers movement (FabLab) to VLSI
  - Open Hardware : Netlist, layout, benchmark are publicly available and may be modified and enhanced with new features
  - Very popular : Arduino PCB

2. `Stallman,FreeSoftwareFoundation,https://www.fsf.org`
3. `Barriga,CSC'17`

OHW definition

What ? Hardware Design using Free and Open Source Tools (FOSS-EDA) and Open Hardware (OHW) "IPs".

OHW should come with a documentation : schematic diagrams, circuit or circuit-board layouts, flow charts and data-sheet, as well as other explanatory material (see CERN).

Open source hardware is hardware whose design is made publicly available so that anyone can study, modify, distribute, make, and sell the design or hardware based on that design (see Open Source Hardware Association)

Why ?

- OHW : to share IPs with community
- FOSS-EDA : to make, reuse, and remake IPs (The Cadence case [4])
- Licences : to be sure that all is free (GPL [5], CERN [6]), Creative Common
- AMS : not only CMOS digital but CMOS analog and Mixed-Signal

4. OpenAccessCoalition,http://projects.si2.org/?page=77
5. GnuPublicLicense,https://www.gnu.org/licenses/quick-guide-gplv3.en.html
6. OpenHardwareLicense,2017,2021,https://cern-ohl.web.cern.ch/

Free versus Open Concepts

Words are confusing :

- Open : Open Source, the "programmer" point of view. The software sources are available.
- Free : from a "societal" point of view. Free as *Liberty*.
- CopyLeft : "In the GNU project, our aim is to give all users the freedom to redistribute and change GNU software. If middlemen could strip off the freedom, our code might "have many users," but it would not give them freedom. So instead of putting GNU software in the public domain, we "copyleft" it. Copyleft says that anyone who redistributes the software, with or without changes, must pass along the freedom to further copy and change it. Copyleft guarantees that every user has freedom."

Free versus Open SW by Stallman

https ://www.gnu.org/philosophy/open-source-misses-the-point.html

Motivation for OHW with FOSS-EDA

- Make : movement attracts people
  - Diversity induces nice ideas : More people, more ideas !
- Democratizing VLSI making
  - SMEs : More chips !
  - More designers : innovation and diversity
- Supporting teaching activities in Universities
- Decreasing the cost of circuit design
  - More design will reach the silicon implementation
- More clients for foundry
  - Motivation for foundry to provide NDA Free access to fabrication
- Creation of benchmark circuits to compare concepts
- Full transparency and control of the design [7]
  - Which has an impact of security

7. Arnd Weber, Steffen Reith, Michael Kasper, Dirk Kuhlmann, Jean-Pierre Seifert, and Christoph Kraub : Sovereignty in Information Technology. Security, Safety and Fair Market Access by Openness and Control of the Supply Chain. 2018. http ://www.QuattroS-Initiative.org/

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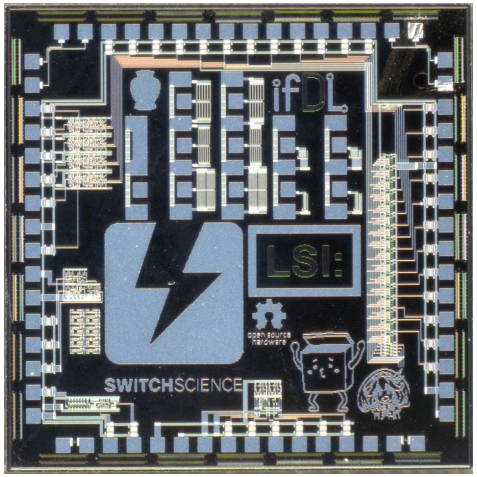
EDA FOSS Examples

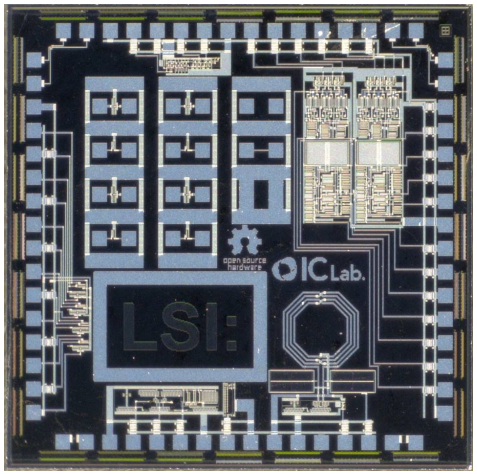
TTool	Embedded Systems, HW/SW Partioning, Verification, L. Apvrille https ://ttool.telecom-paris.fr/index.html
SystemC AMS	System simulator released by COSEDA
IEEE 1666.1	http ://www.accellera.org/downloads/standards
SpinalHDL	High Level Language for Digital design by Charles Papon https ://spinalhdl.github.io/SpinalDoc-RTD/
GHDL	VHDL simulator by Tristan Gingold https ://ghdl.readthedocs.io/en/latest/
YOSYS	Gate level Digital Synthesis by C. Wolf http ://www.clifford.at/yosys/about.html
ngspice	Circuit simulator by Holger Vogt https ://sourceforge.net/projects/ngspice/
Coriolis	VLSI backend, by LIP6 https ://www-soc.lip6.fr/en/team-cian/softwares/coriolis/
Chips4Makers	Standard Cell library by Staf Verhaegen https ://chips4makers.io/blog/
KLayout	GDS viewer and editor by Matthias Koefferlein http ://www.klayout.de/index.php

Plan

Use Cases - MakeLSI : Project



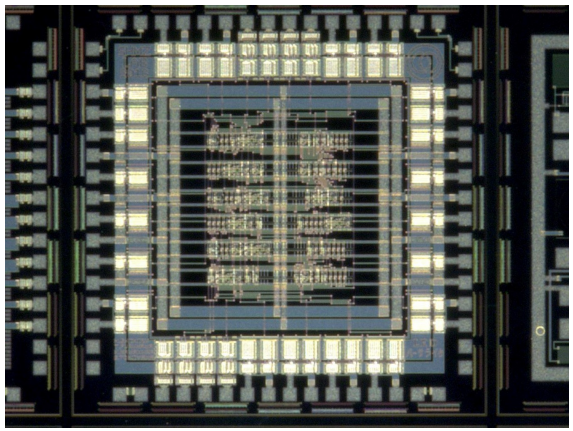
AMS CMOS chip1



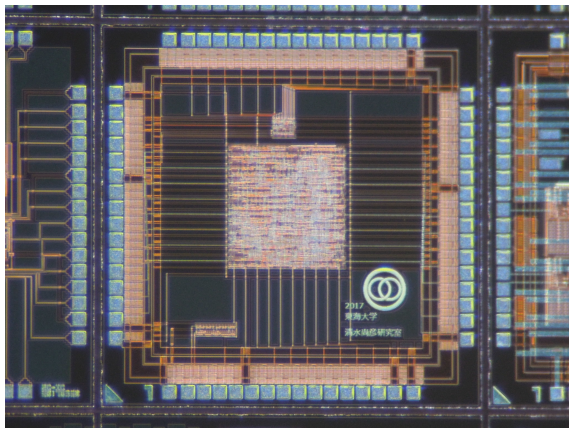
AMS CMOS chip2

- Pr. J. Akita is leading the project at Kanazawa University.
- NDA free process.
- Fabrication at "Foundation for the Advancement of Industry, Science and Technology" (FAIS) facilities, or others.
- Node 1μm FAIS.
- Using Open Source tools (Wgex and Glade).
- 4 year running, AMS circuits.
- 14 circuits from 12 participants (researchers & amateurs)
- MOSFET TEGs, VCO, Guitar amplifier.

Use Cases - MakeLSI : Project (Continued)



Chip with FAIS technology



Chip with Phenitec technology

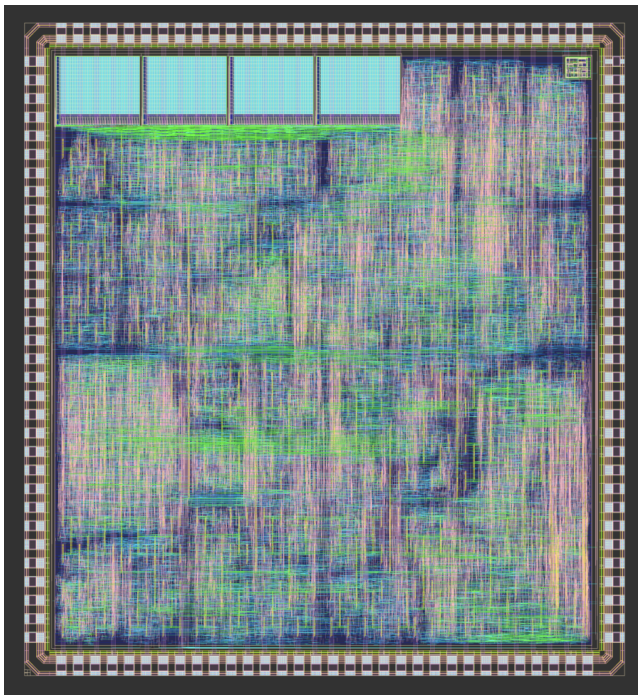
- Pr Naohiko Shimizu (Tokai University)
- Node 1μm FAIS.
- Made with FOSS EDA Alliance (digital) symbolic.
- Non NDA free technologies used :
  - 0.6μm Phenitec,
  - 180nm ROHM.
- Micro-controllers, but AMS is on-going project.
- Symbolic approach allows layout exchange.

Flow Assembly

Tool interoperability is illustrated by the following flow :

1. nMigen (https://github.com/m-labs/nmigen)
2. GHDL (Tristan Gingold)
3. Yosys (C. Wolf).
4. c4m-flexcell (FibraServi, Staf Verhaegen)
5. Coriolis (Sorbonne Université-CNRS/LIP6)
6. KLayout (Matthias Koefferlein).

Use Cases - LibreSoC : P&R with FOSS-EDA Coriolis [8]



Layout with Coriolis2
Standard Cell Library :
c4m-flexcell

Libre-SOC's 180nm Power ISA Test ASIC :

- developed in conjunction with Chips4Makers and Sorbonne Université's LIP6,
- submitted to Imec's MPW Shuttle Service for fabrication in TSMC 180nm,
- founded by NLnet foundation,
- see https://libre-soc.org/

8. https://openpowerfoundation.org/libre-soc-180nm-power-isa-asic-submitted-to-imec-for-fabrication/

And the others ?

USA initiative :

PDK without NDA by Google and Sky Water CMOS 130nm :
https://skywater-pdk.readthedocs.io/en/latest/status.html

The Open Road Project :
https://theopenroadproject.org/

FOSSI Foundation :
https://www.fossi-foundation.org/

In France and in Companies too !
Thales is a strategic member of the RISC-V foundation :
https://riscv.org/about/

Plan

Towards an Open Hardware Licence

Reminder ...

- I am not a lawyer
- This section is based on the presentation by Tristan Gingold from CERN [9] at FSIC 2019, [10]
- The CERN OHL is based on the documents by Javier Serano, from CERN Open Hardware Licence, OHL v2 [11]

9. https://home.cern/fr
10. https://wiki.f-si.org/index.php/CERN_OHL_v2_draft
11. https://ohwr.org/project/cernohl/wikis/Documents/CERN-OHL-version-2

Why a Licence from CERN ?

See Tristan Gingold presentation at FSIC 2019

- CERN designs many electronic boards
- Some of them are general-purpose (ADC, PCI, ...)
- Some are needed in large amount
- Produced by external companies (manufacturers, foundries)
- Increasing the market size will reduce the price
- CERN needs a Licence !

Why an Open HW Licence ?

See Tristan Gingold presentation at FSIC 2019

- CERN is funded by public money
- Knowledge dissemination is part of their mandate
- An open license is a *natural way* to disseminate HW.

The CERN Open Hardware Licence

It aims at providing a solid legal basis for the sharing of hardware designs. In this release (v2), CERN intends to give Licensors different options for the sharing mechanism : strongly reciprocal, weakly reciprocal and permissive.

Why not using a FOSS Licence, like GPL (or CC) ?

See Tristan Gingold presentation at FSIC 2019

- GPL is well known and tested in courts

But HW designers use (have to use) :

- Proprietary tools and file format
- Proprietary/Patented IP cores
- *Copying* is understood (several ways ...)
- *Running* is not meaningful/well defined
- Building the product is the essential goal

An Open Licence

See Tristan Gingold presentation at FSIC 2019

The freedom :

- Copy and distribute copies of sources
- Modify the sources
- Distribute your changes
- Make and distribute the product

and the consequence

But you must keep –information, legal– notices, and provide the sources.

The complex heterogeneous product (with HW)

See Tristan Gingold presentation at FSIC 2019

The product can be :

- A bitstream (for an HDL design)
- A mounted PCB (for an electronic design)
- A device (for a ready to use design)
- A 3D printed object
- An ASIC

CERN has the goal to be as general as possible (consider all cases).
Does it work for your domain ?
Addressing : Designers, Makers, Manufacturers.

Strong and Less

- CERN-OHL-S is a strongly reciprocal licence. For example, if you release HDL files under CERN-OHL-S and then somebody uses those files in their FPGA, when they distribute the bitstream (either putting it online or shipping a product with it) they need to make the rest of the HDL design available under CERN-OHL-S as well.
- CERN-OHL-L is a weakly reciprocal licence. For the example above, if you release your part of the design under CERN-OHL-L, somebody who distributes a bitstream which includes your part does not need to distribute the rest of the design files as well.
- CERN-OHL-P is a permissive licence. It allows people to take your code, relicense it and use it without any obligation to distribute the sources when they ship a product.

Plan

Our Goals

- Provides a platform for academics to allow them to make algorithmic exploration or any experiment.
- Give the ability to publish, share, replicate experiments and modify the hardware design down to the layout.
- Attempt to open the ASIC market to SME.
- Allow a better management of security issues.
- Ensure the continued existence of the hardware.

Short Terms Objectives & Collaborations

- Run on mature nodes. That is above 130nm.
- More specifically, AMS 350nm and TSMC 180nm.
- One tapeout in July 2021 with TSMC, for the first prototype of the Libre-SOC free processor.
- One tapeout in November 2021 using AMS, by Staf VERHAEGEN for the Chip4Makers project.
- A long standing collaboration with Pr. Naohiko SHIMIZU which has made designs with Phenitec 0.6μ, ROHM 180nm and with the free and educational facility of Hibikino 2μm.

Challenges

- A new business model for EDA companies is needed
  - And new jobs and new markets will arise ...
- Continuous and quick maintenance and debugging is required
  - Otherwise ... the tool may become obsolete
- FOSS-EDA and OHW must be extensively verified and validated before usage
  - Otherwise ... the users will loose confidence
- Foundries will have to open their PDK
  - Otherwise ... only old and obsolete technologies will be available
- Funding of Opensource project is not straightforward
  - Academia cannot support all the work on its own

Acronyms

ams : Analog and Mixed Signal
CMOS : Complementary Metal Oxide Semiconductor
DRM : Design Rule Manual
DSP : Digital Signal Processor
EDA : Electrical Design Automation
e-FPGA : embedded Field-Programmable Gate Array
FOSS : Free and Open Source Software
HW : Hardware
IP : Intellectual Property
MPW : Multi Project Wafer
NDA : Non Disclosure Agreement
NOC : Network On Chip
PDK : Process Design Kit
RTL : Register Transfer Level
SoC : System On Chip
SMEs : Small and Medium Enterprises
SPI : Serial Peripheral Interface
SW : Software
UART : Universal Asynchronous Receiver Transmitter