Institut
Mines-Telecom

Why chips drive you nuts?

Chadi Jabbour

Une balade dans le marché aux puces!!

17 November 2022

Disclaimer

The seminar

This seminar will skim over a diversity of topics,

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- to complete my explanations
- and to correct me if i am say bullshit which happens very often

Outline

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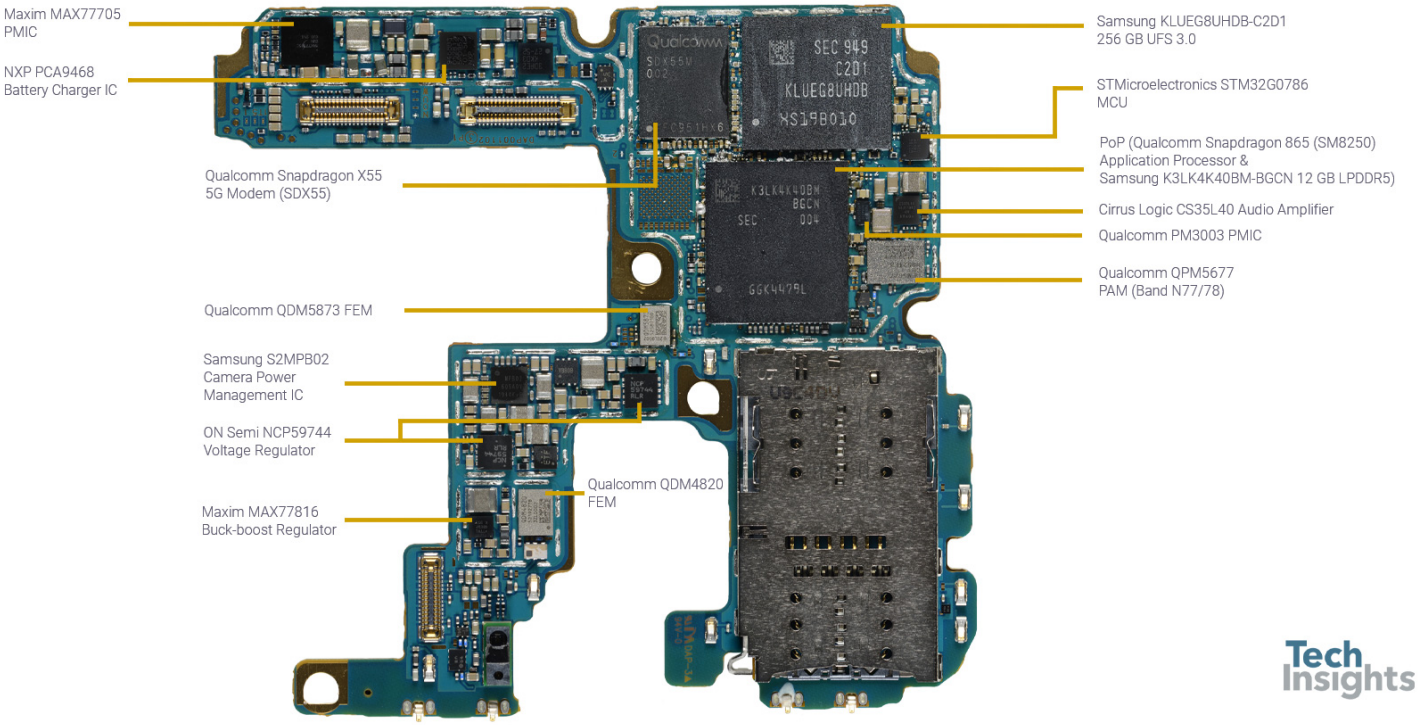
Integrate Circuit (IC), what for?

Samsung S20 mother board



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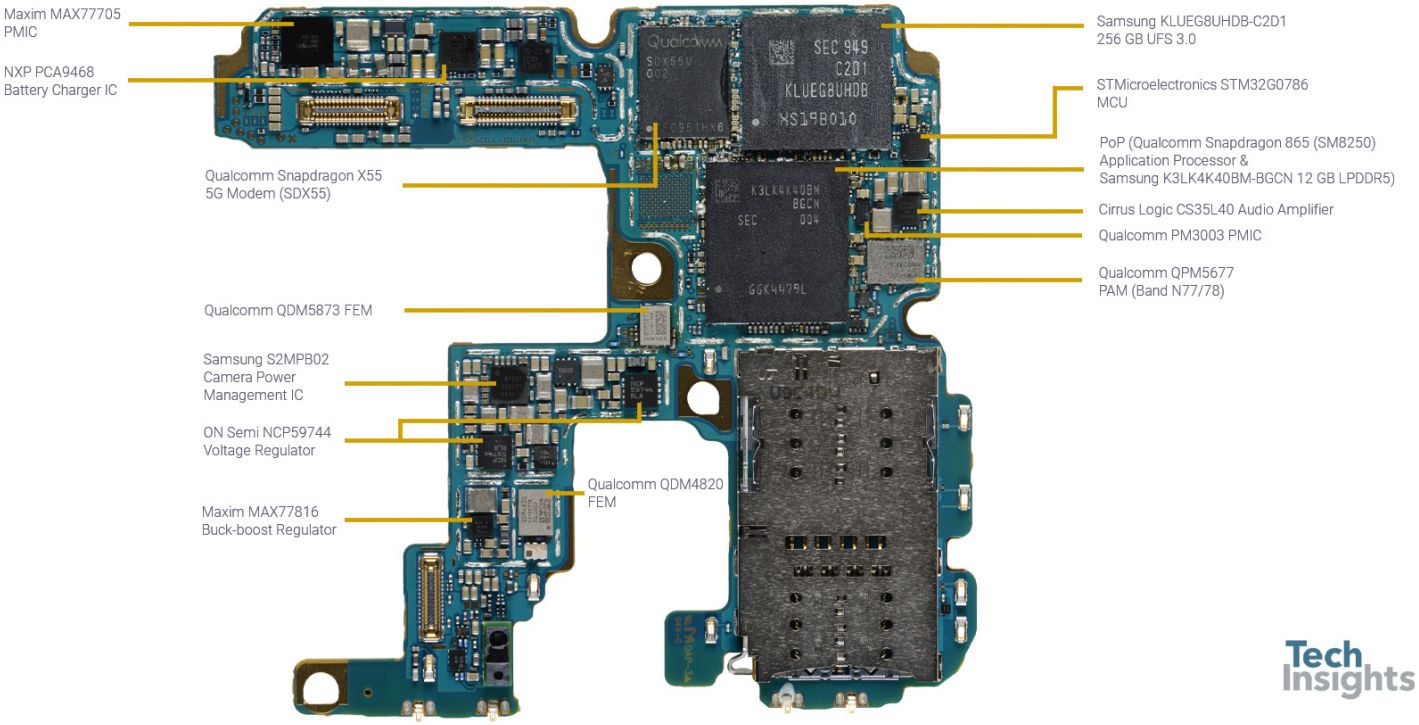

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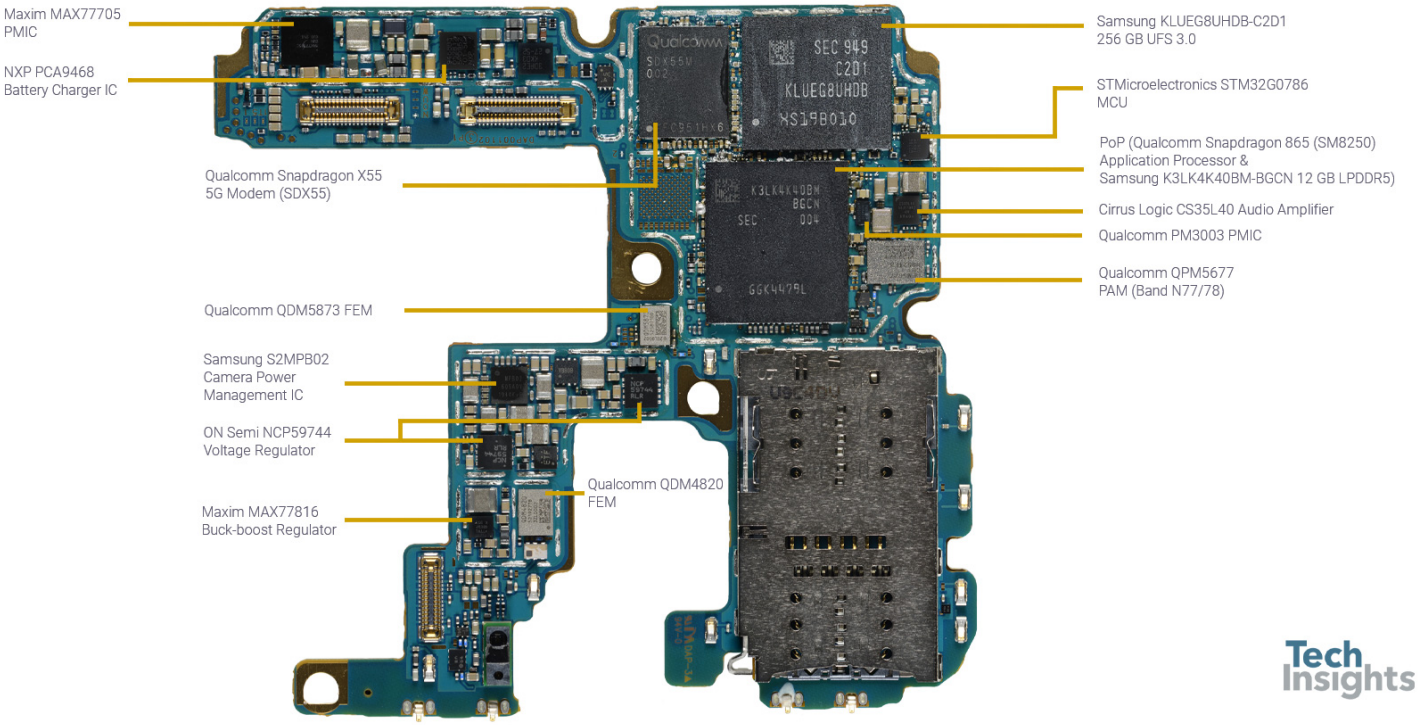

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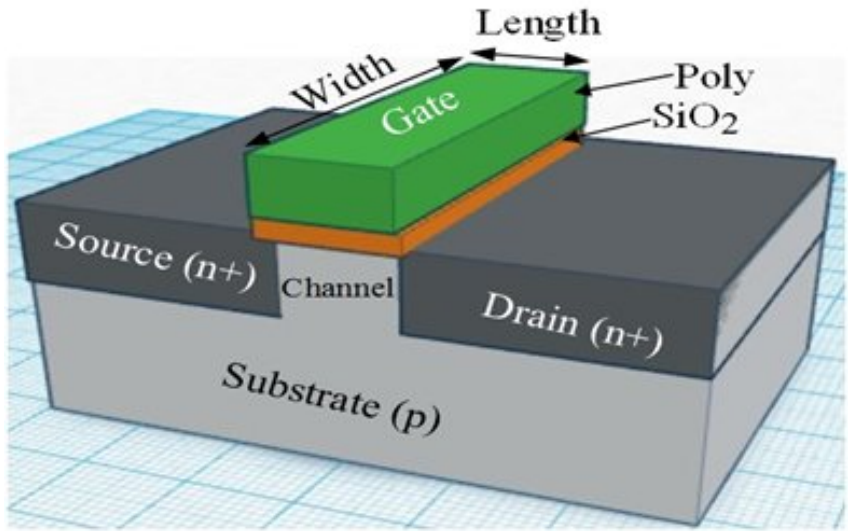
The most dominant technology for IC design is CMOS but others such AsGa, GAN or SiGe are used for high power high frequency RF applications

Technologie CMOS

Transistor NMOS (Negative channel Metal Oxide Semiconductor)



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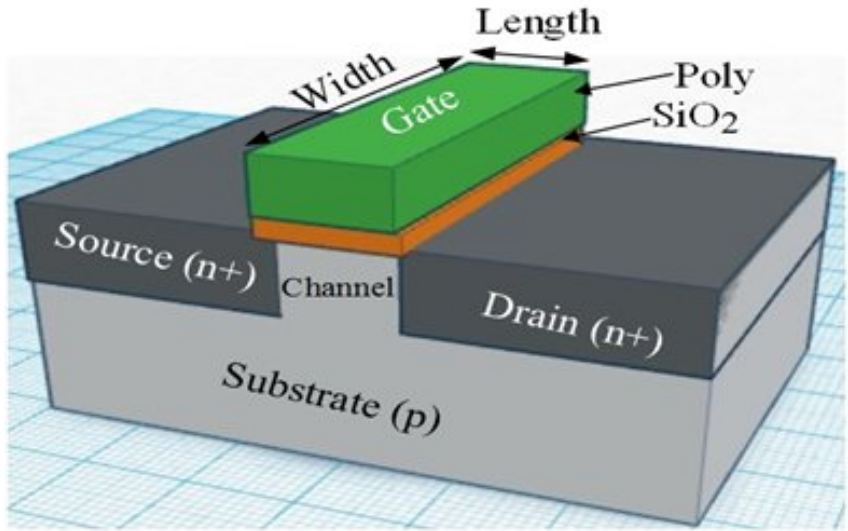
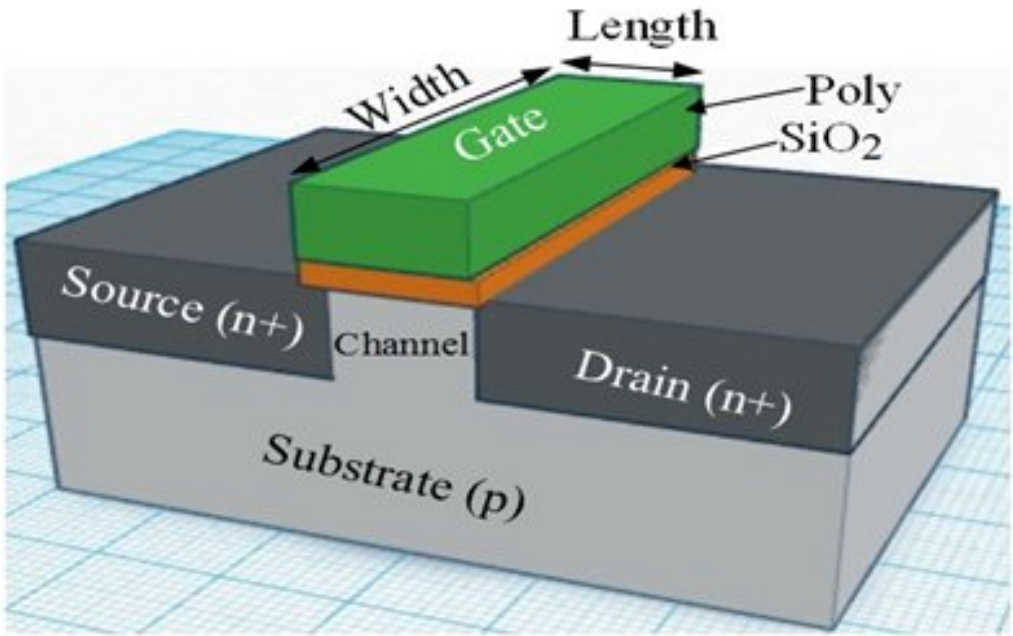


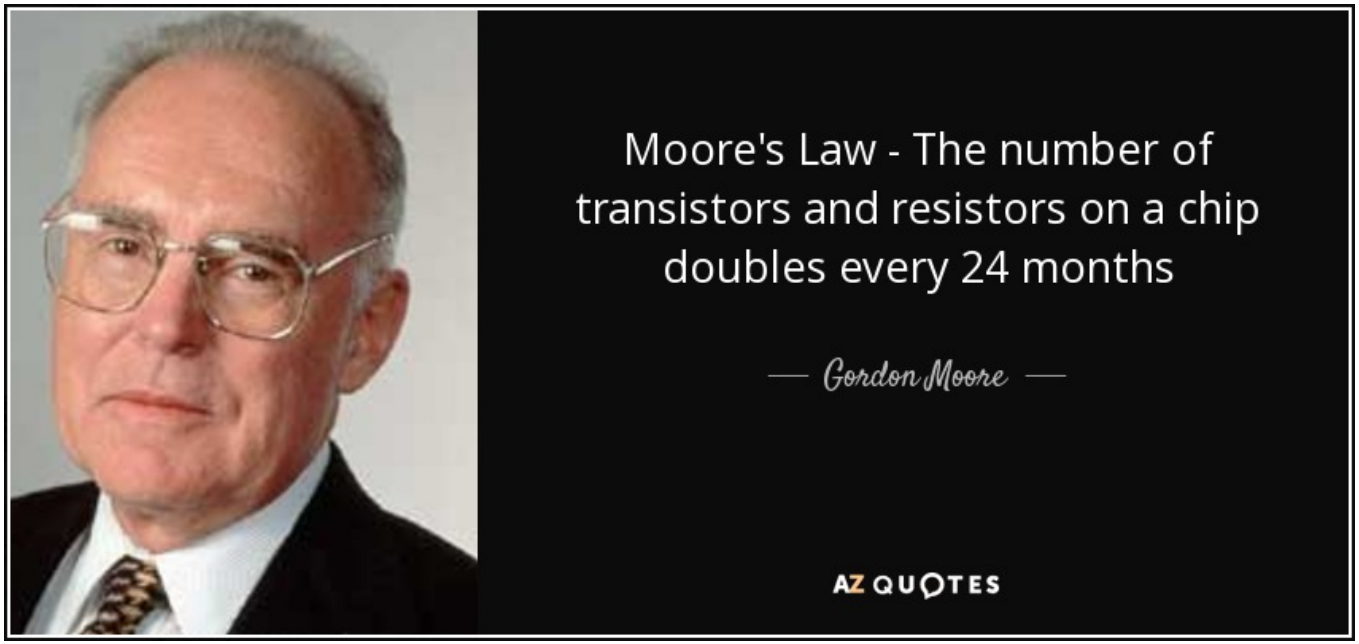
- Depending on the gate, source and drain voltages, the NMOS transistor behaves either as a closed or open switch, or as a current source controlled by V_{gs}
- The PMOS transistor has the same behavior as the NMOS but reversed (P+ diffusion areas in an N- substrate)
- The combination of the 2 types of transistors gives us the "Complementary Metal Oxide Semiconductor" or CMOS technology

Technologie CMOS



- When refering to a 40 nm CMOS technology, 40 nm refers to the channel length
- The transistor parasitic capacitors and thus power consumption are proportional to $W \cdot L$
- While its speed is approx. proportional to $\frac{W}{L}$

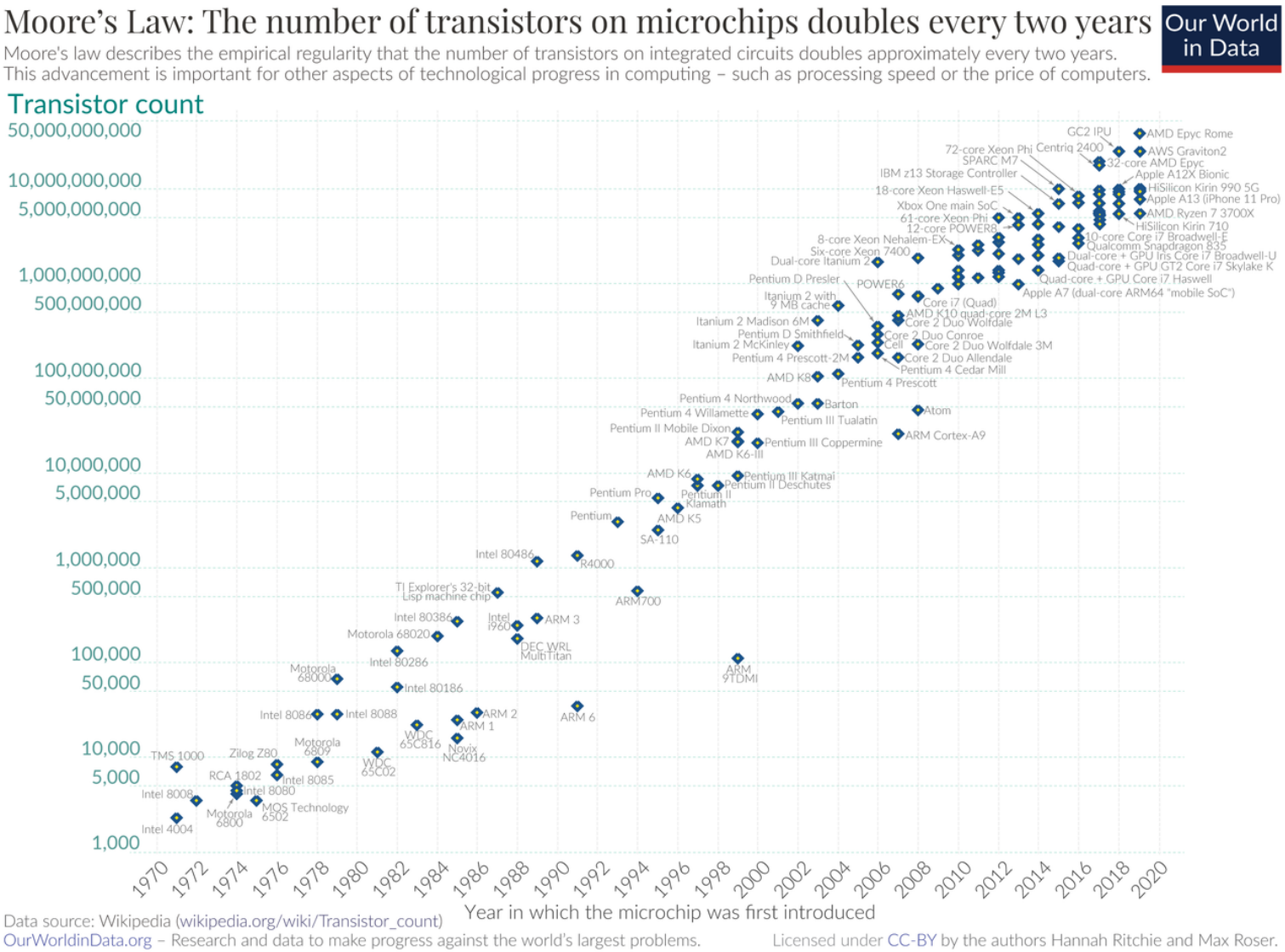
Moore' law - 1965



Gordon Moore

Co-founder of Intel in 1968 with Robert Noyce and Andrew Grove

Number of transistors in a processor



Moore's law consequences

If in a given surface, we want to double numbers of transistors:

- A $\frac{W}{L}$ constant, L must $\searrow \sqrt{2}$ from one technology node to the next so that the surface ($\propto W \cdot L$) $\searrow 2$ every 2 years

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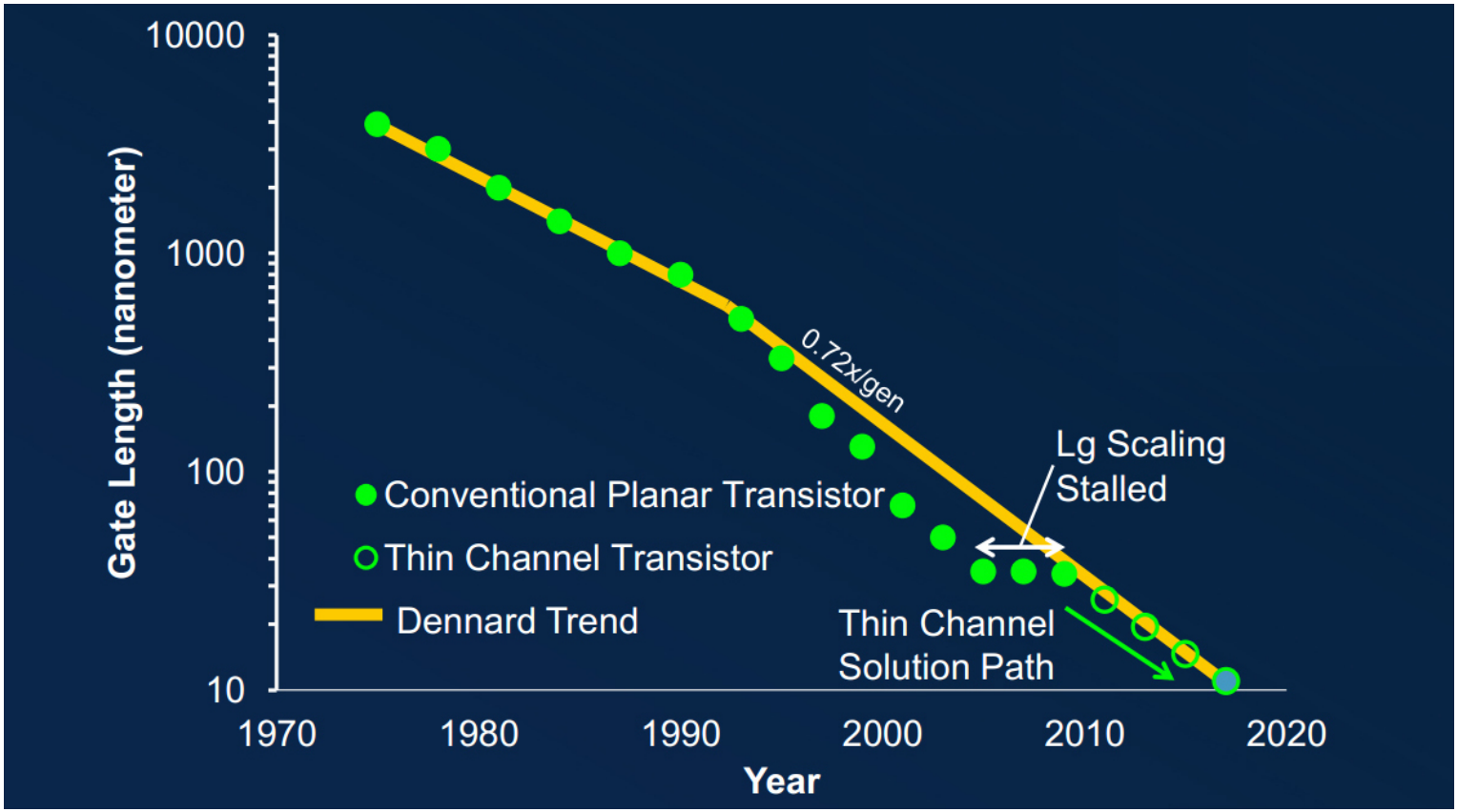
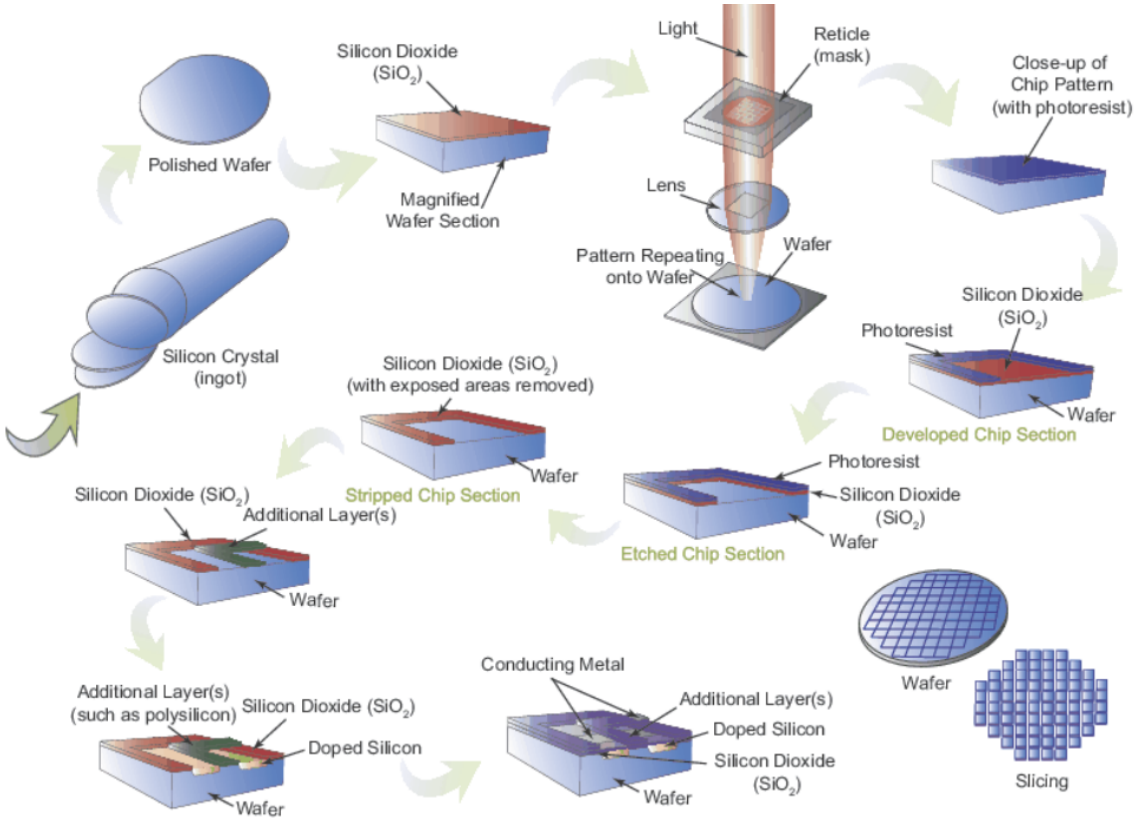


[source: Applied Materials]

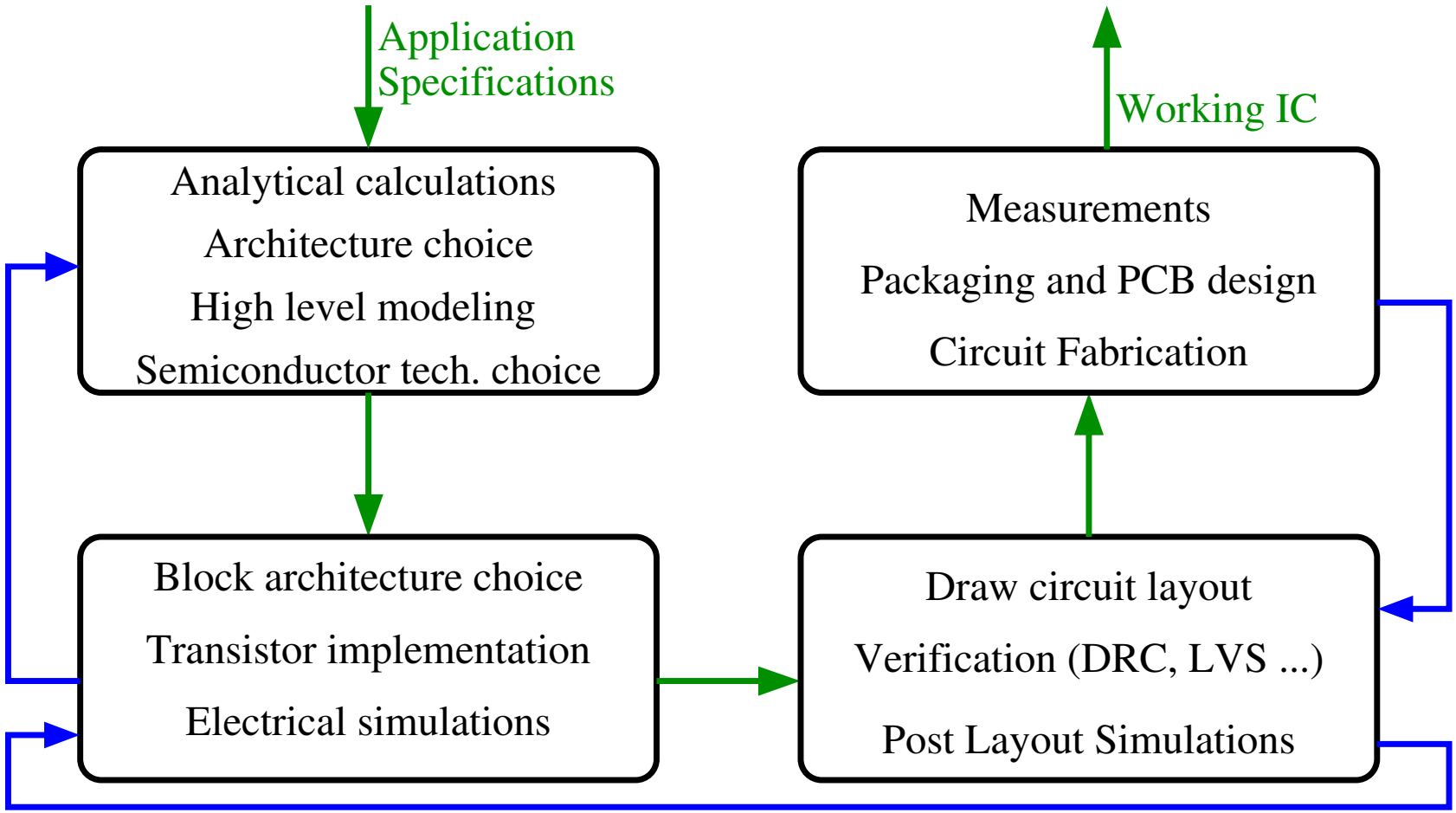
Manufacturing process



IC manufactring is long (6 to 12 weeks), very expensive and integrates many risks

Outline

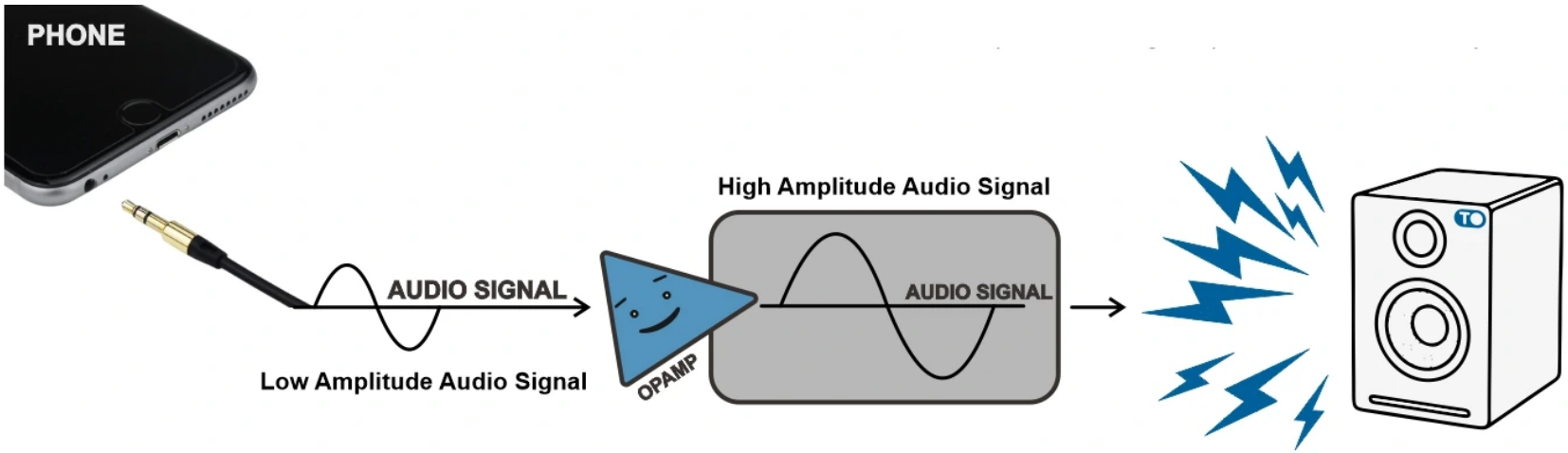
Analog Design Flow



Example - Specifications

We need an audio amplifier with

- A gain of 10
- A bandwidth of 20 kHz
- An SNR of 100 dB
- ...



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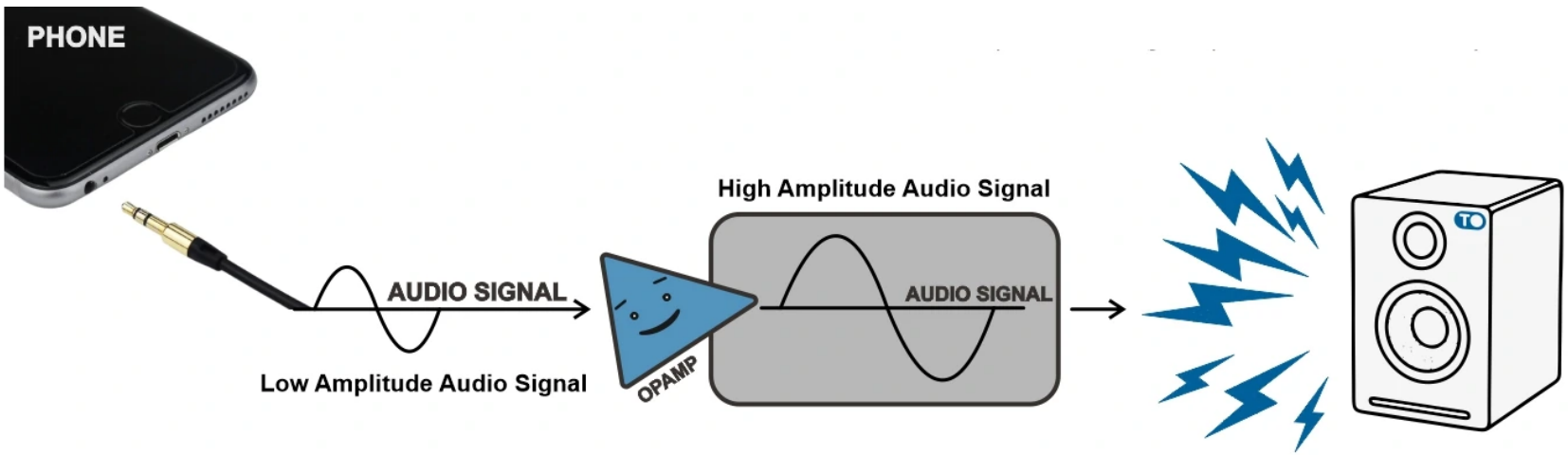
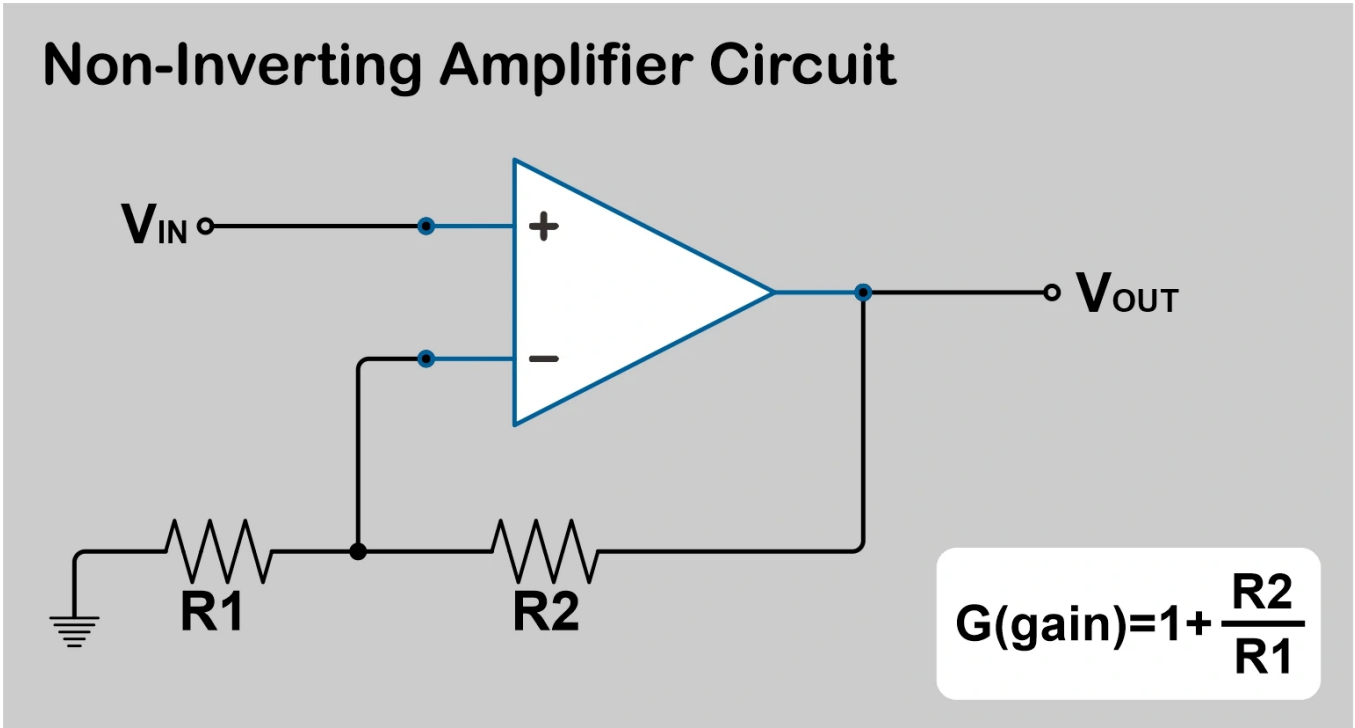


Amplifier schematic

Assuming an ideal operational amplifier



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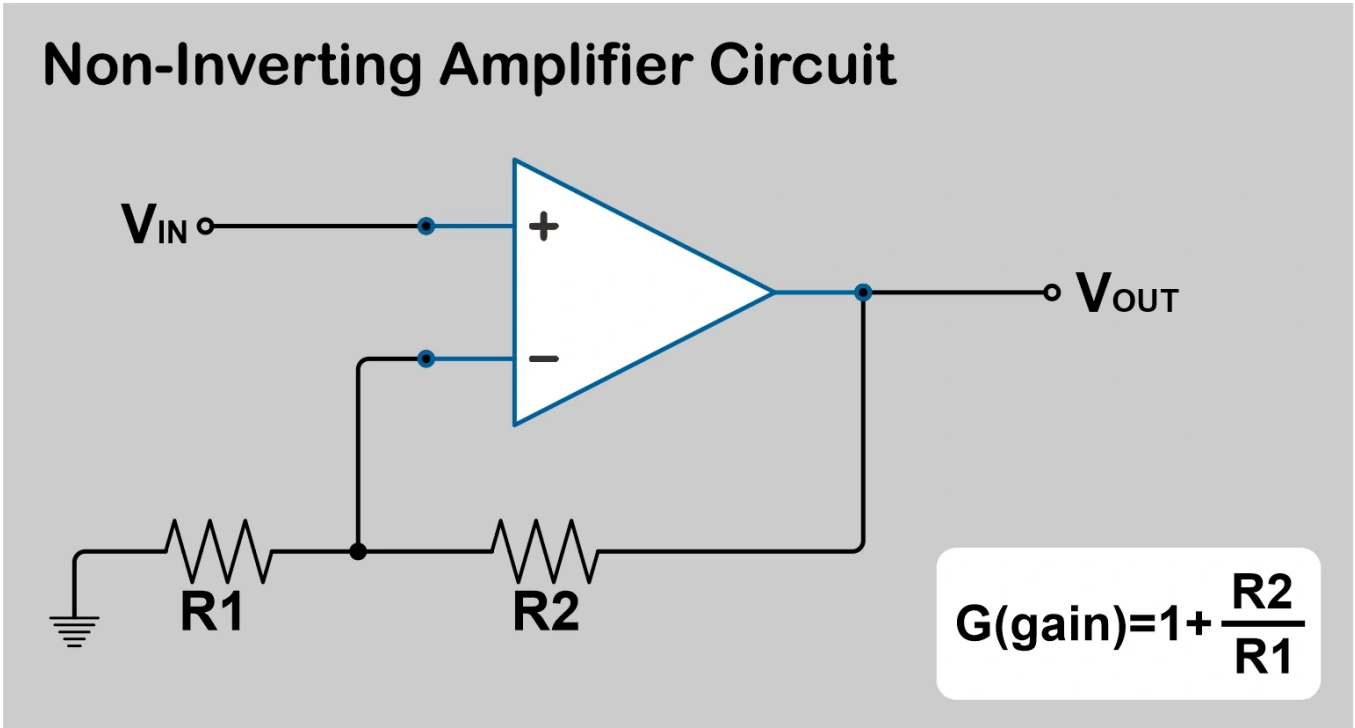

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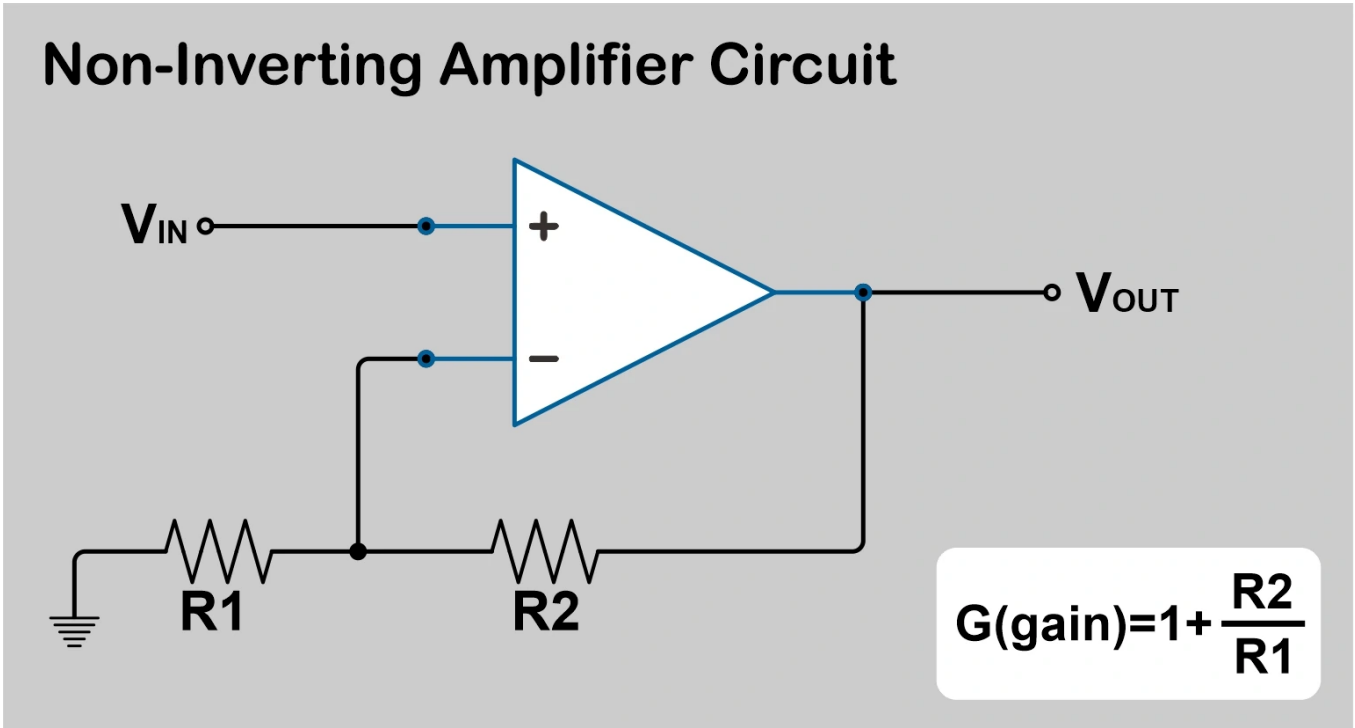

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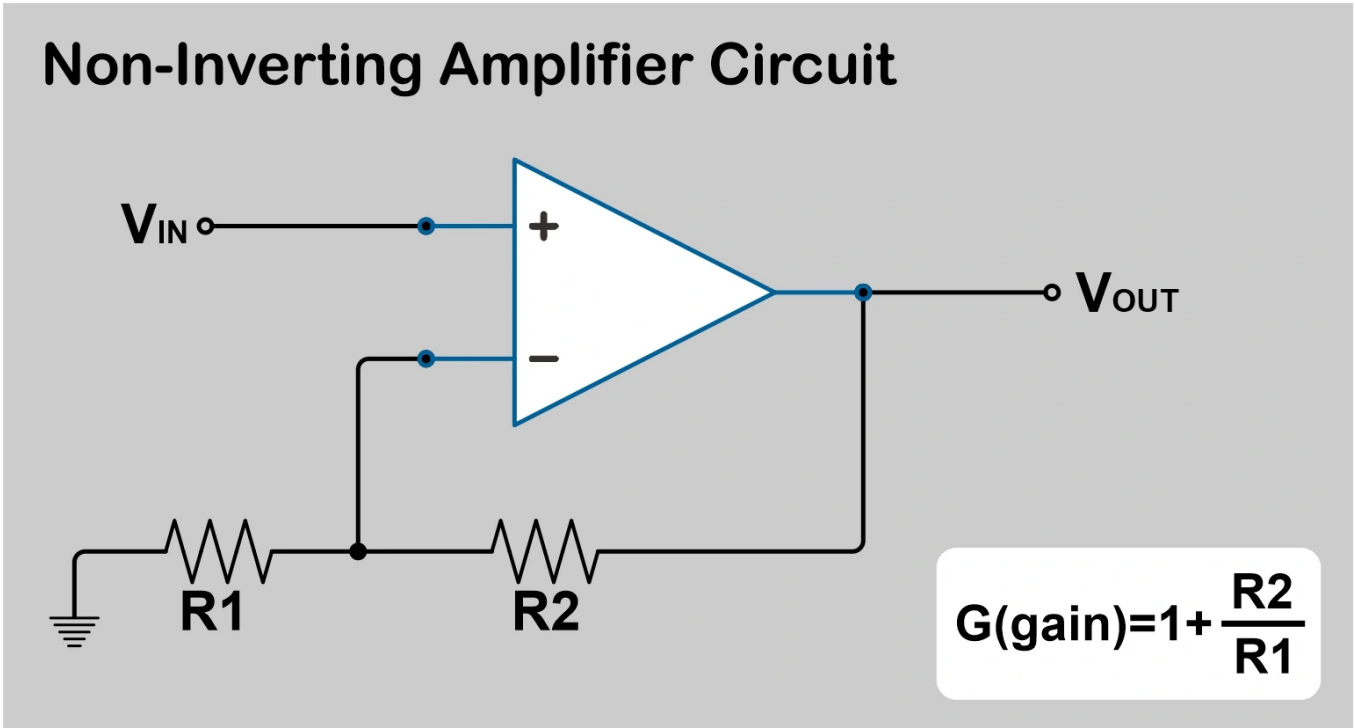

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We will actually find the specifications for the operational amplifier which allow to achieve the targeted gain with enough precision

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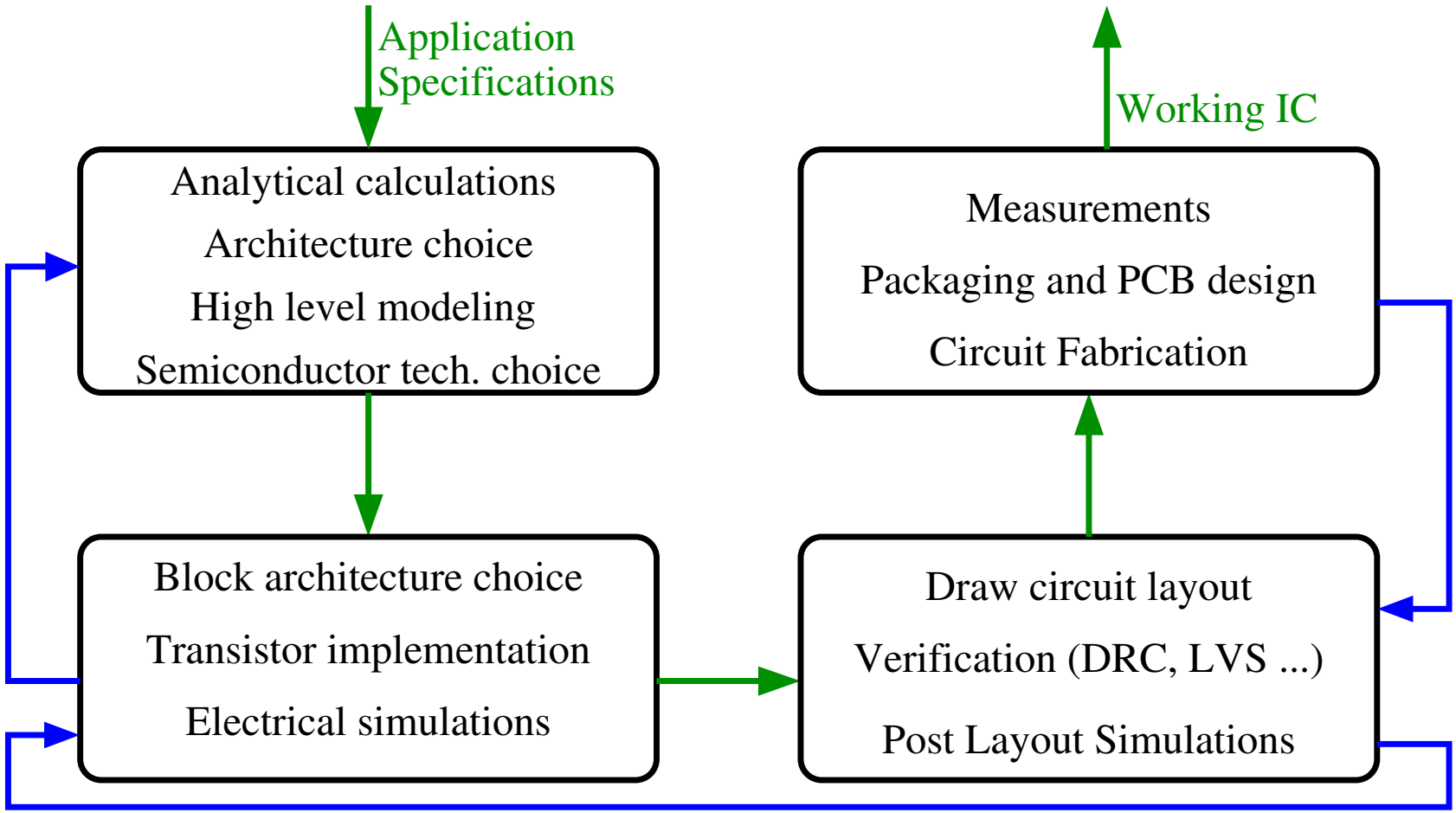

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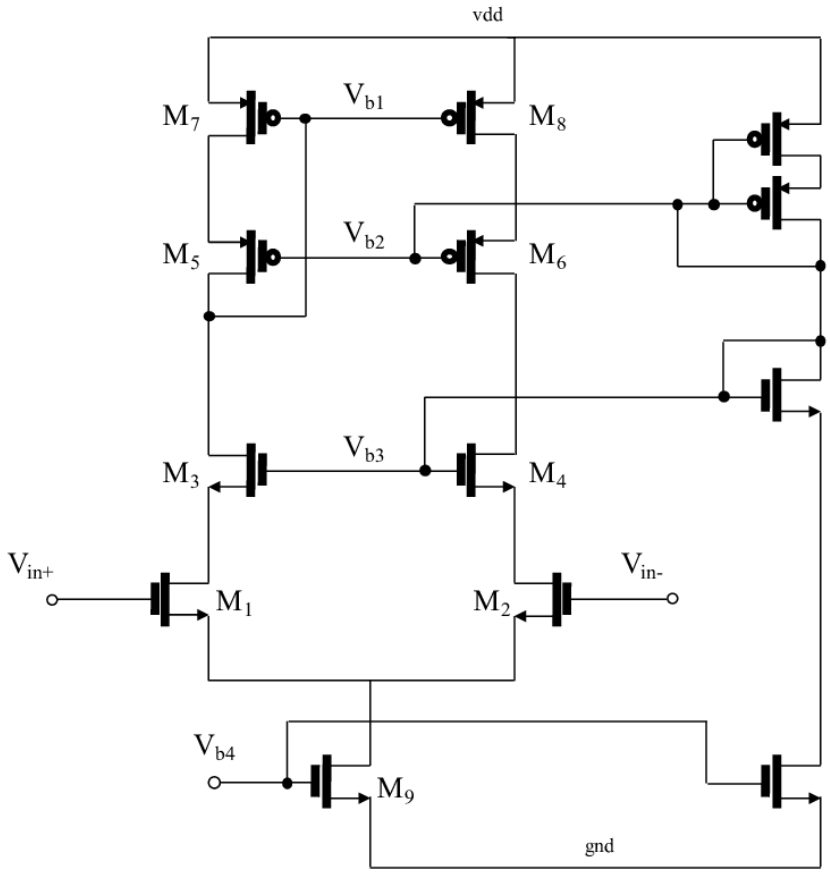

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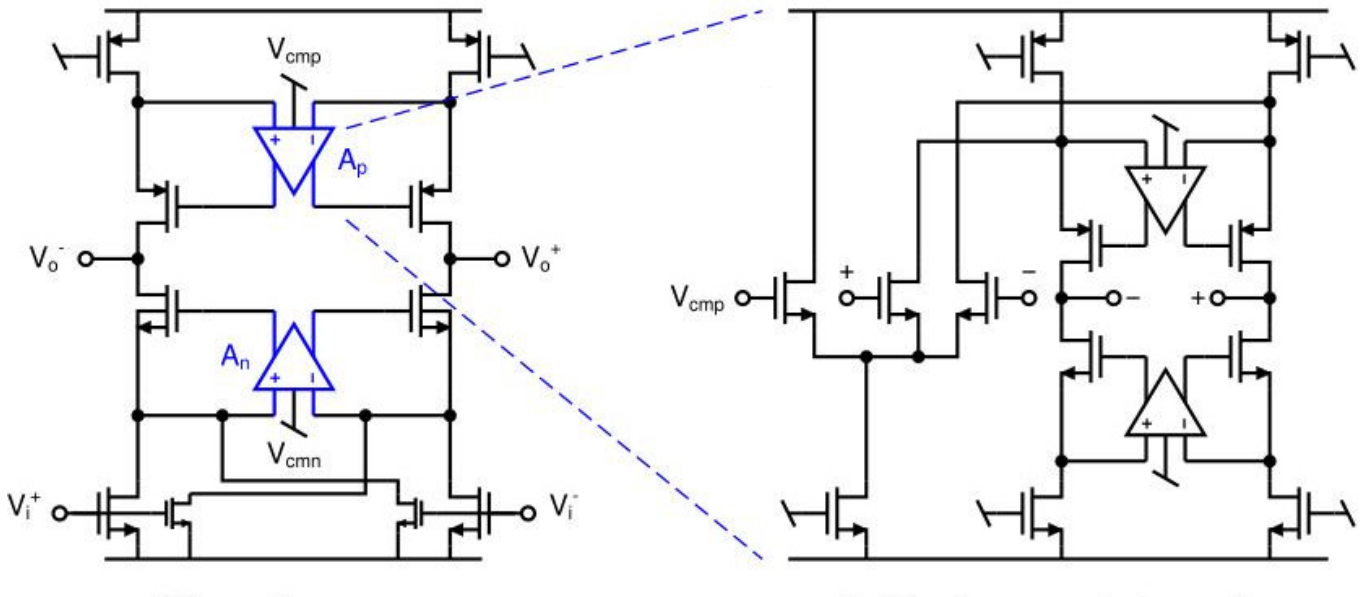

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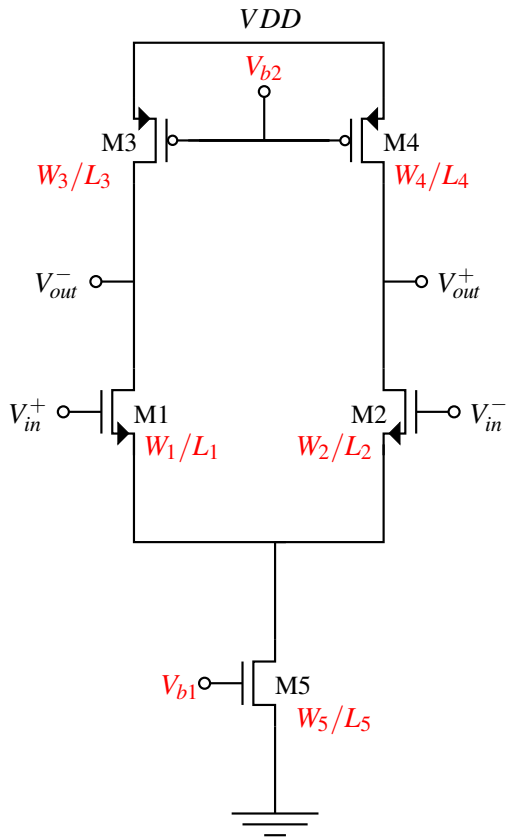

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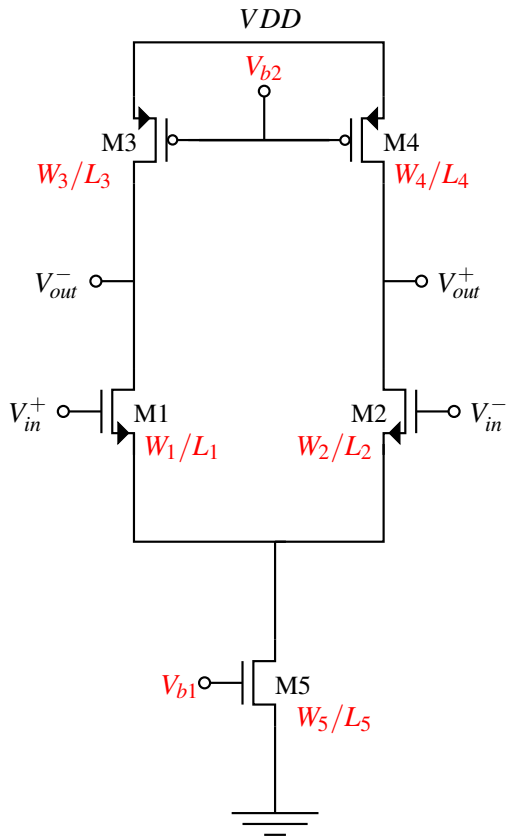

So basically we need to find the sizes of the transistors ($W_{1\to5}$, $L_{1\to5}$) and the bias voltages V_{b1} and V_{b2}

Amplifier sizing

The design/sizing is a very time-consuming task, it is guided/done

- Based on the understanding of the circuit and/or

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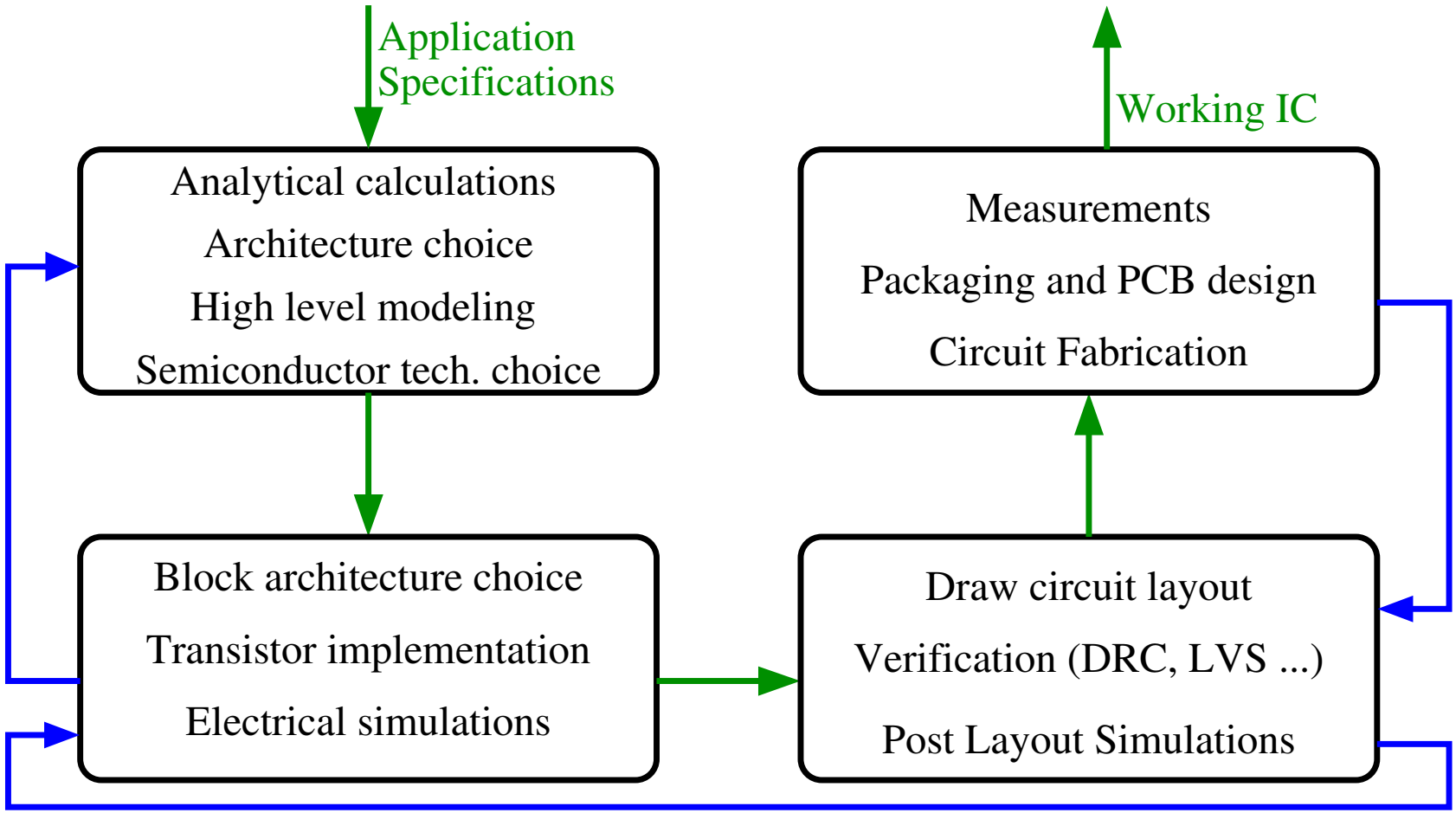
- IA because it is the solutions for the all the problems

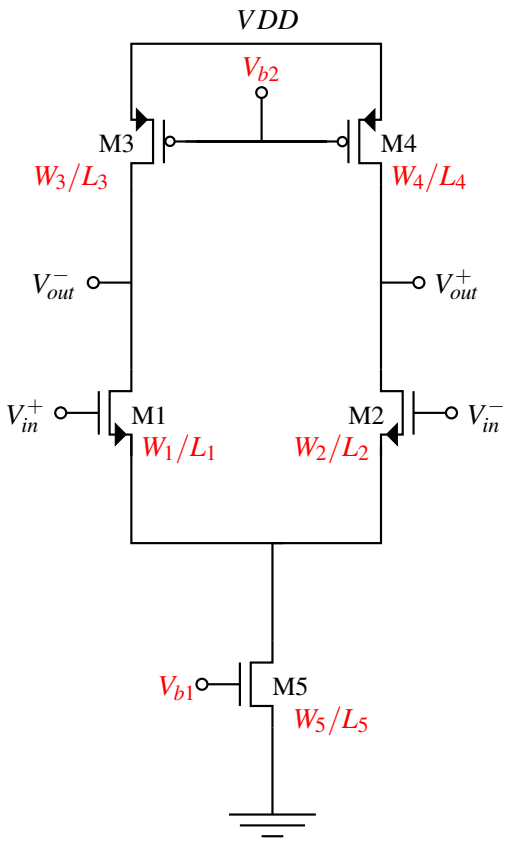
The electrical simulators

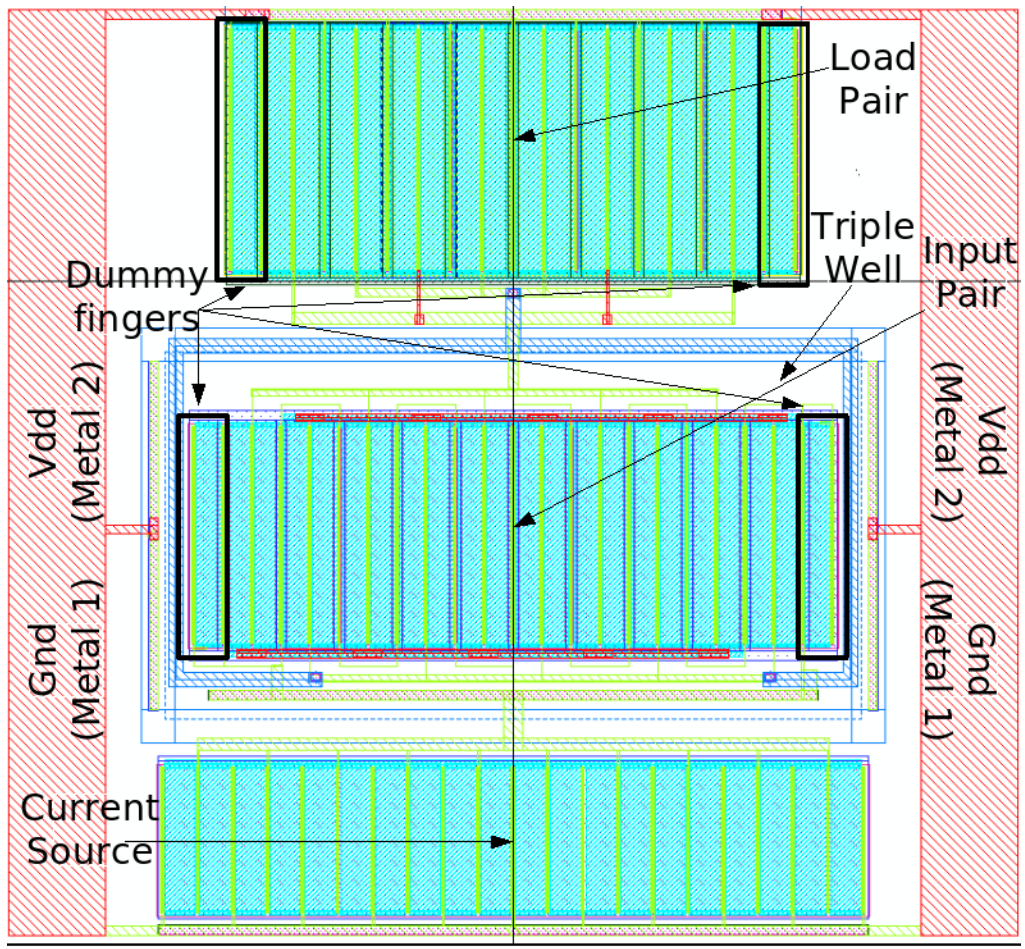
- An electrical simulator is a class of software that simulates the behavior of electrical circuits
- Difference with a simple programming language (C, python, Matlab ...)
  - is able to emulate simultaneous simulation
  - is able to emulate continuous time simulation
  - allows to obtain info for both voltage and current
- Simulators allows to integrate the transistor models provided by foundries
- Industrial design suites (CADENCE, MENTOR) are very expensive ($\sim$ 50 k€ per year per licence)

Analog Design Flow



Layout



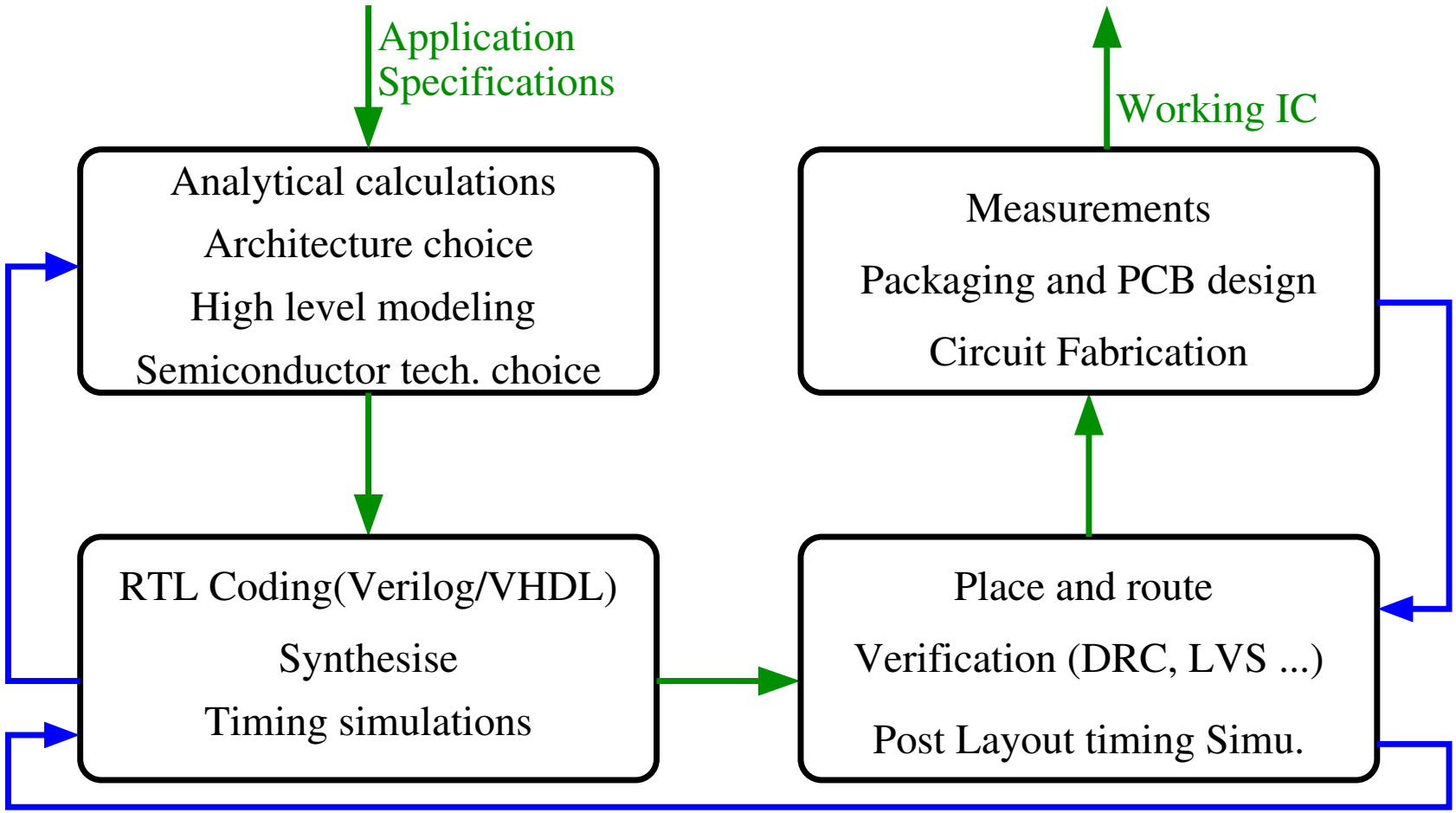


Analog Layout is often done by hand and needs to follow lots of rules of performance (IR drop, coupling, matching, ...) and manufacturability (diodes, mechanical stress, latchup)

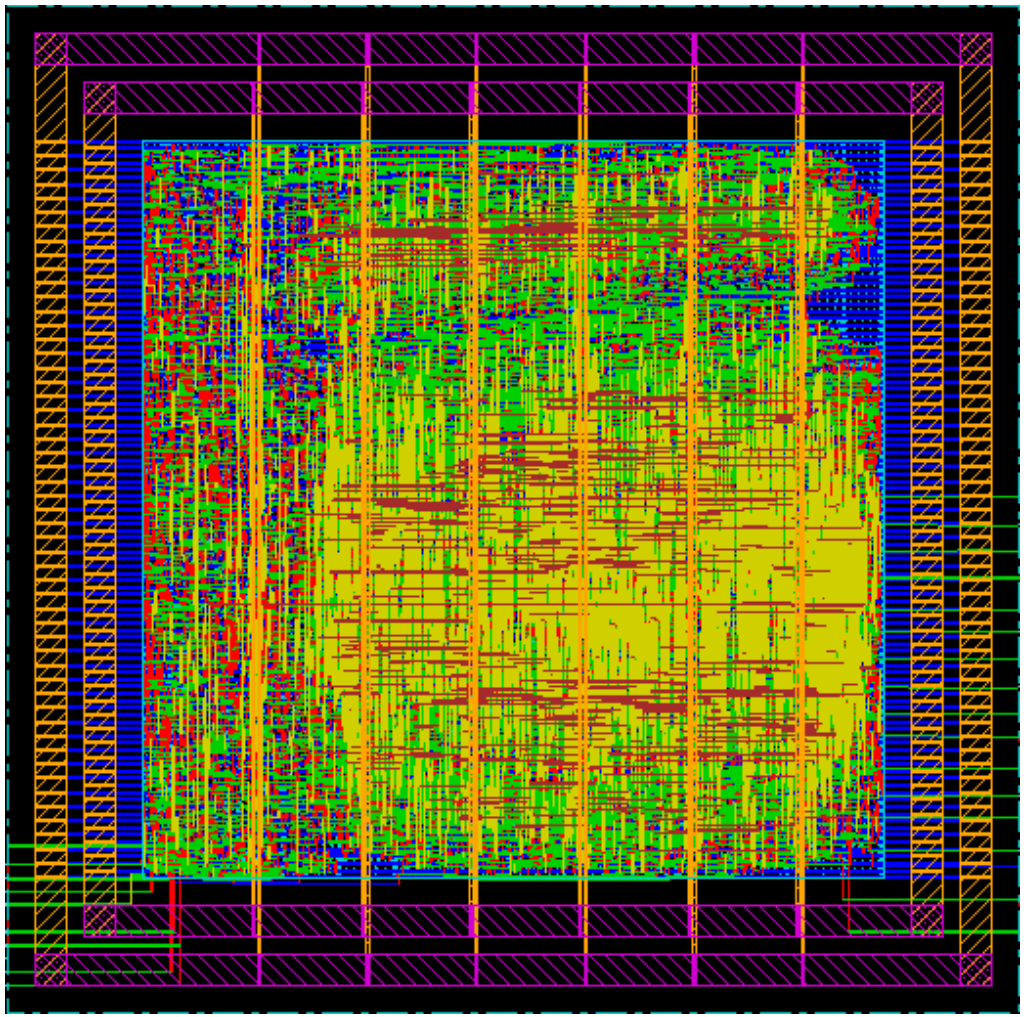
Constraints

- The transistor models are getting more and more complex (several thousands lines of coding), analytical calculations are becoming less and less accurate
- The IC components suffer from a 3-σ 15 to 20 % variation, design margins and/or calibrations are needed
- Electrical simulations are very long, can take several days/weeks for complex systems. Multi-level modeling, clever choice of simulations
- Electrical simulations are not always fully reliable because not all the aspects are well-modeled, the simulator resolver can mess around ...
- Layout adds parasitic resistances and capacitors that should be extracted and new simulations should be carried out

Digital Design



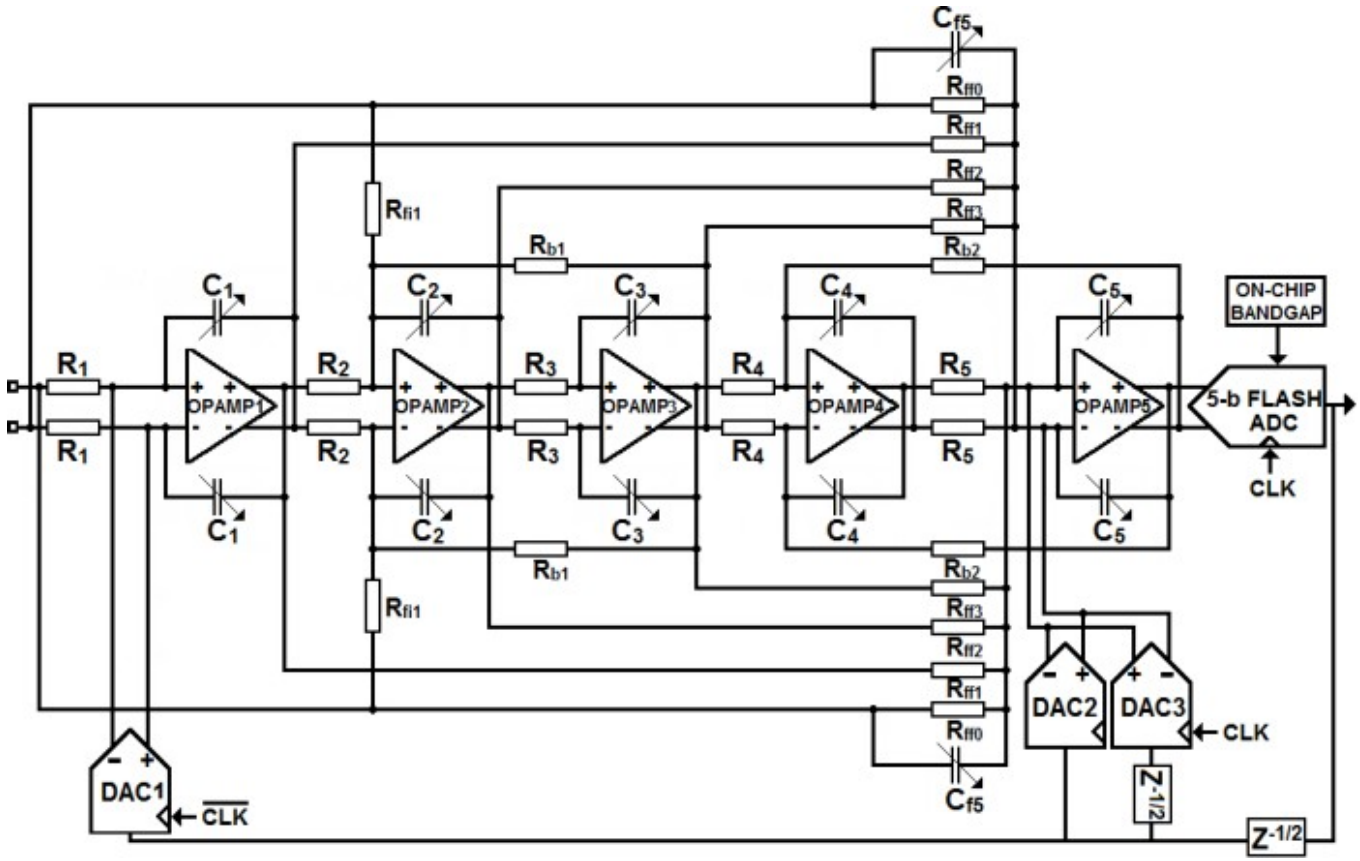
Example with a digital filter



- Around 8000 digital gates, more than 100000 transistors
- Synthesized, laid out and Simulated in less than 20 minutes

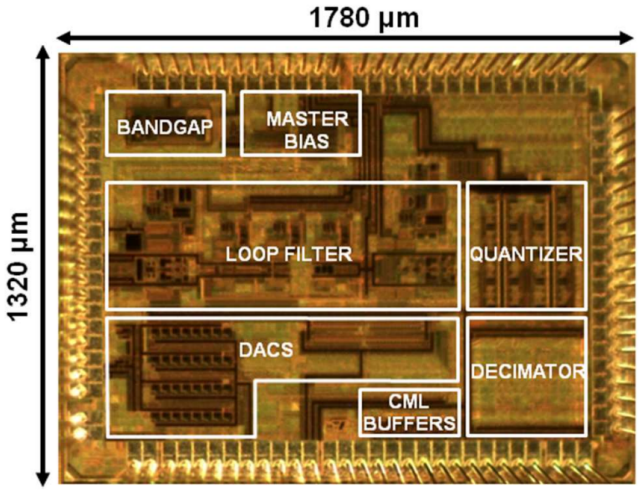
Outline

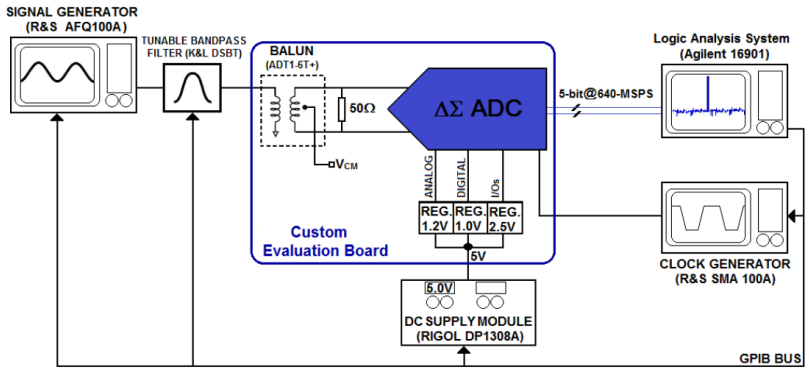
CRIOS Data Converter



- A 11-bit 80/40/20 MS/s 5^{th} order OSR-8 $\Delta\Sigma$ ADC
- IC half way between a prototype and a product as it integrates on chip calibrations, decimator and bandgap

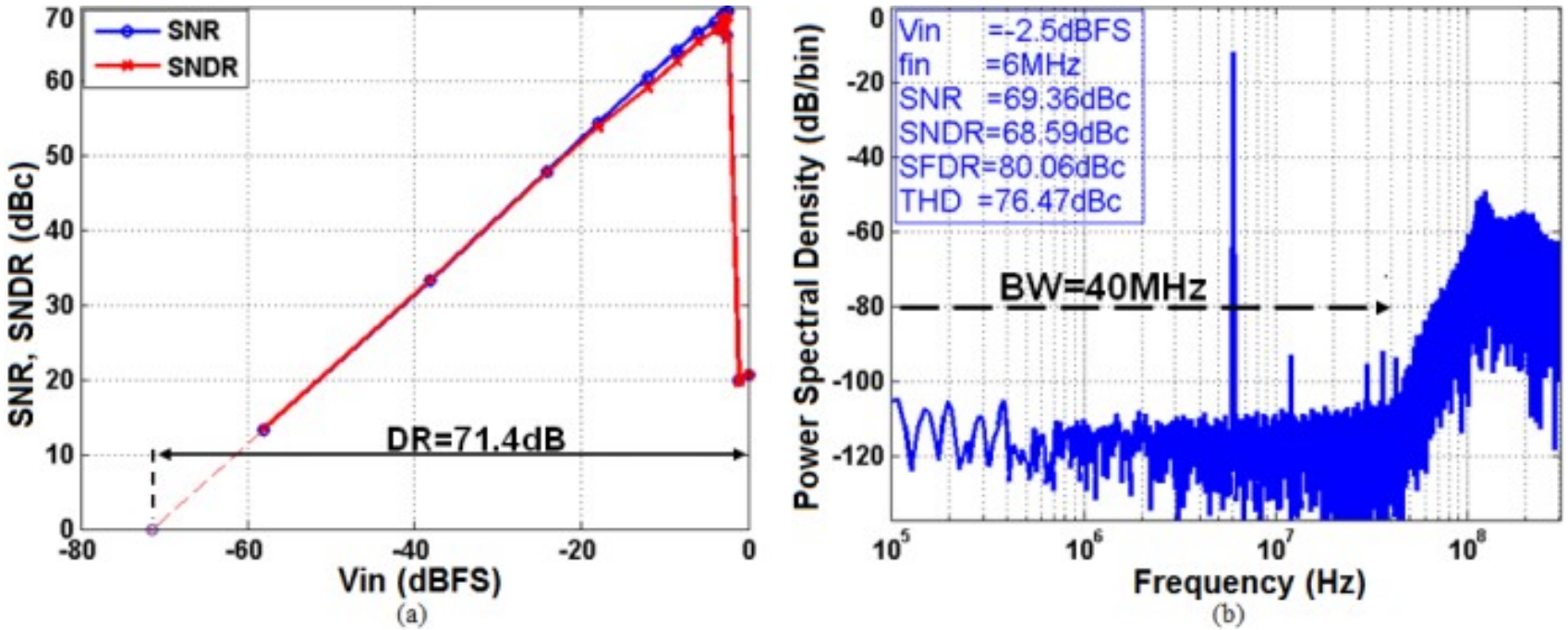
Chip Mircograph





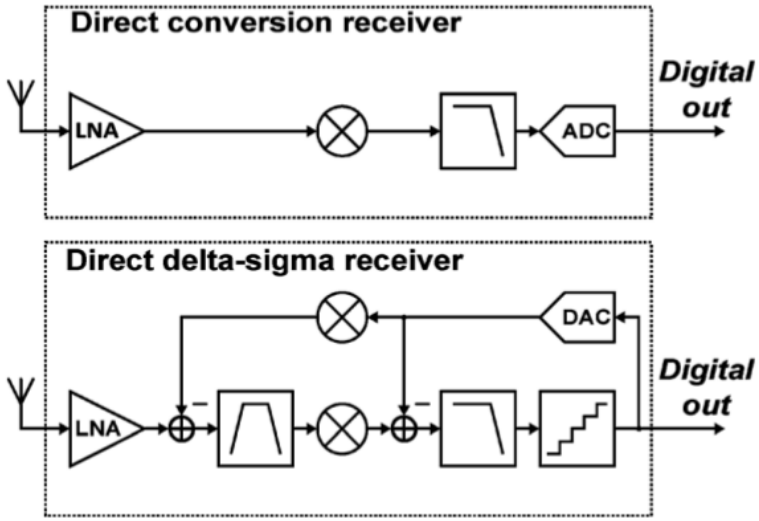
- The circuit was fabricated in a 65 nm CMOS from STMicrolectronics
- Its area is around 2 mm^2 and was encapsulated in a 100-pin Ceramic Quad Flatpack (CQFP) package

Measurement results



- ADC achieves 11 bits of resolution, 72 dB of Dynamic range with a power consumption of 82.3 mW
- It was the founding stone to start SCALINX in 2015

DDSR vs conventional receiver



Main advantages of the RF feedback

- Relaxing the linearity requirements as the signal swing is reduced
- Increasing the Noise Transfer Function order

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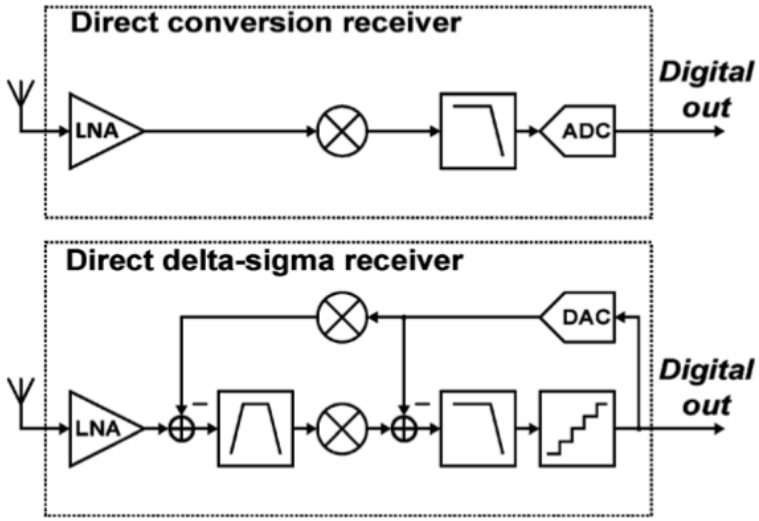

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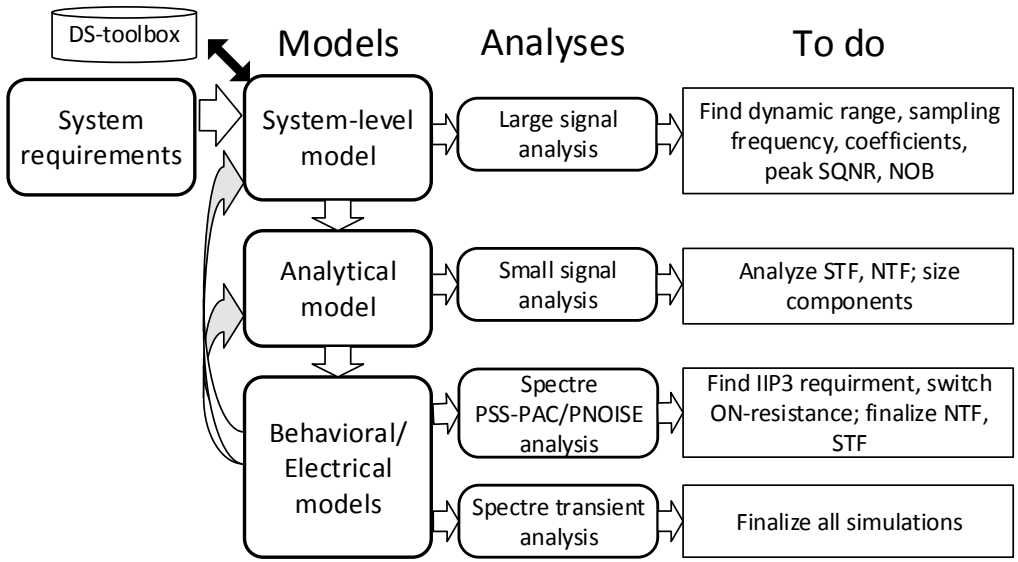
Main challenges in the architecture

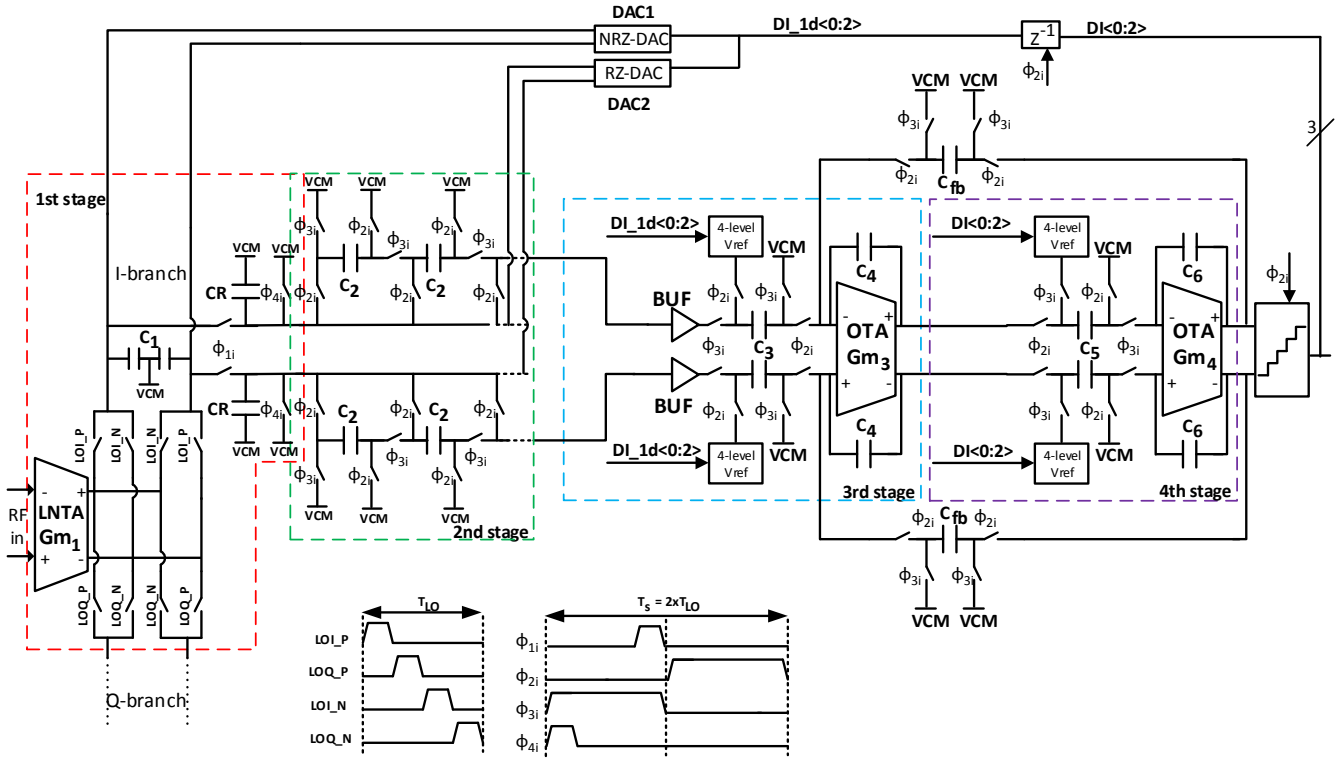
- The conventional design approaches can not be applied directly to the DDSR
- Noise coupling due to the RF DACs

Top-down modeling and analysis approach for DDSR design.



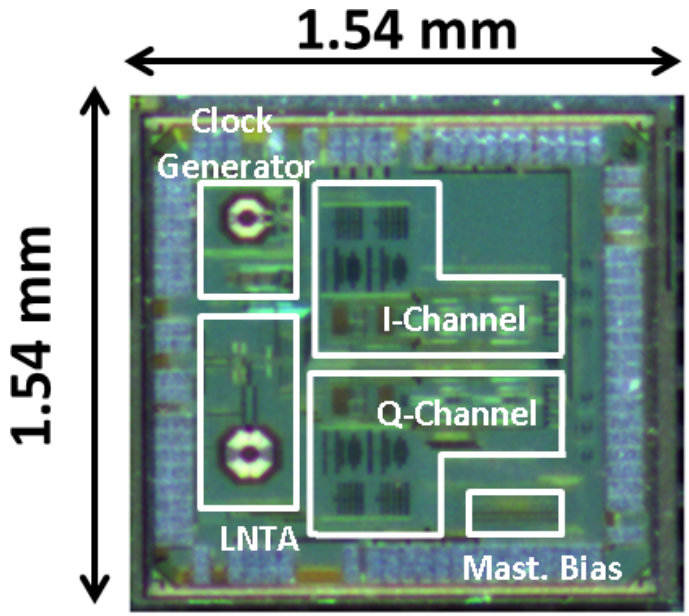
System-level	Analytical model	PSS-PAC/PNOISE	Transient
1.0 mins	0.25 mins	0.5 mins	9.2 mins

Proposed 0.4-6 GHz 4th-order DT-DDSR



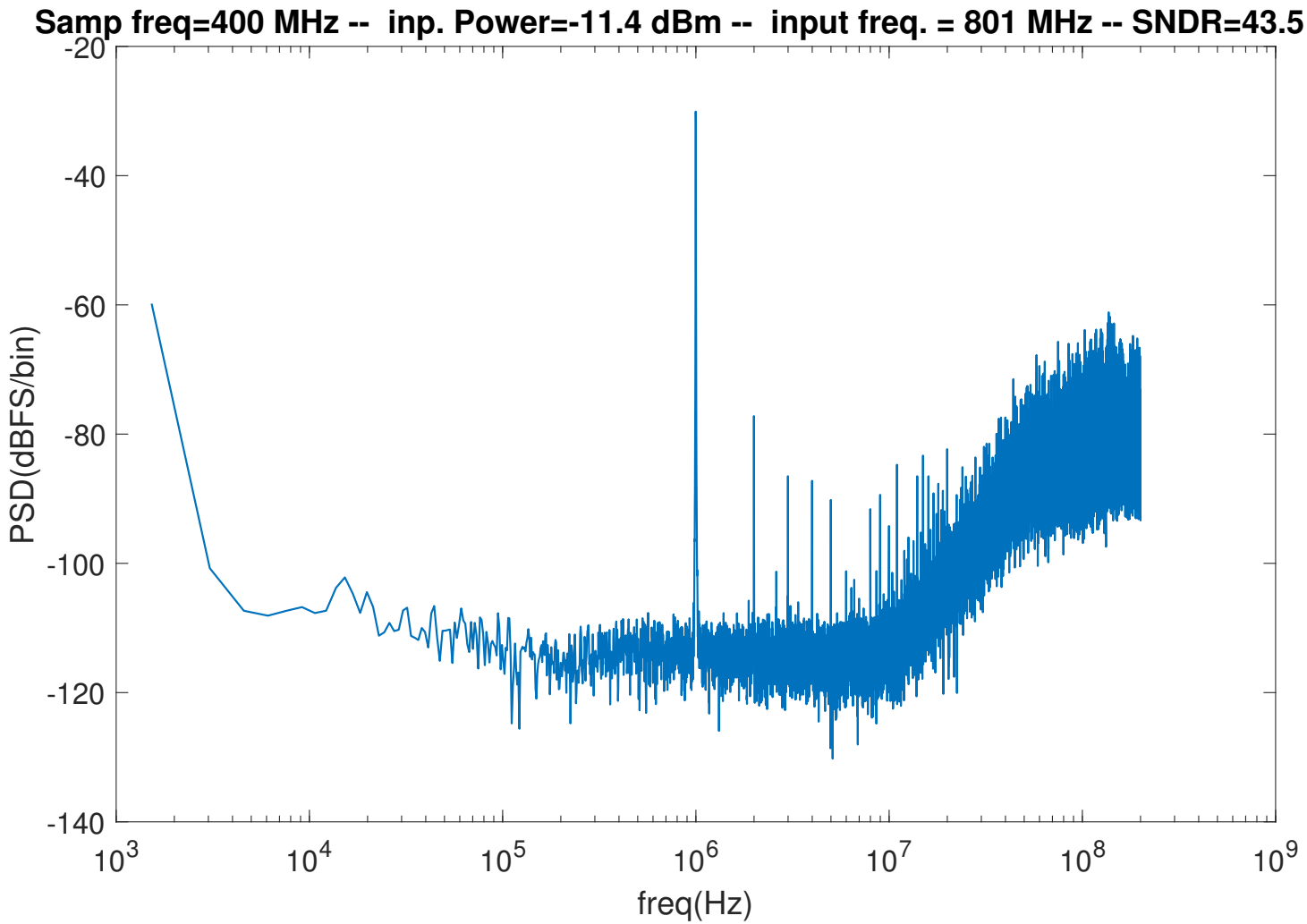
- Uses an f_s as a divider of f_{LO} which avoids quantization noise folding and allows to use one coefficient set
- Uses a DT passive/active architecture to reduce power consumption

DDSR Die photo



- 65 nm CMOS process from STM encapsulated in a 80-pin QFN package
- The 400 MS/s I/Q channel outputs are driven out using CML buffers

Measurements results



PSD with a clock division by 2 - a SNDR of 43 dB

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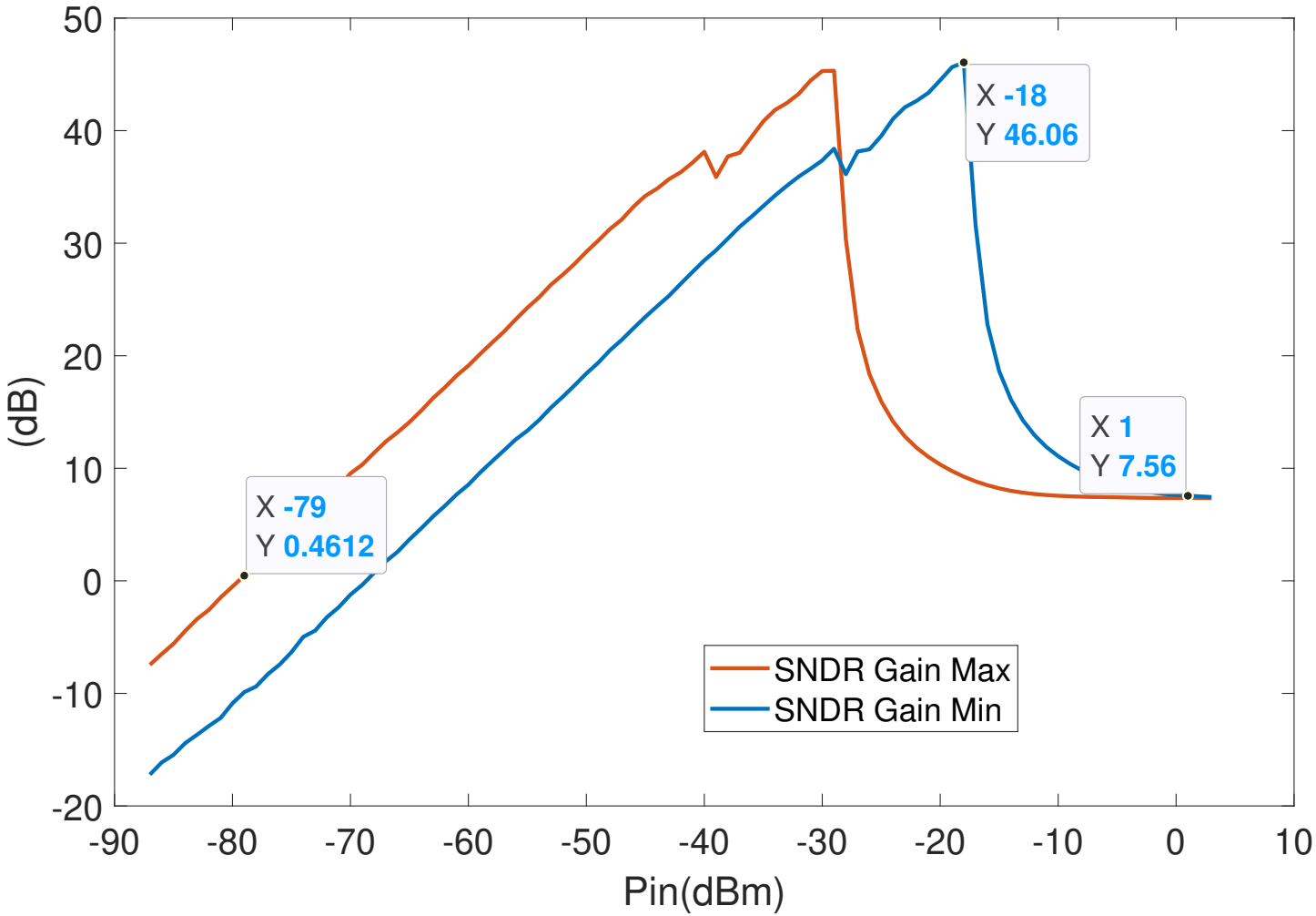
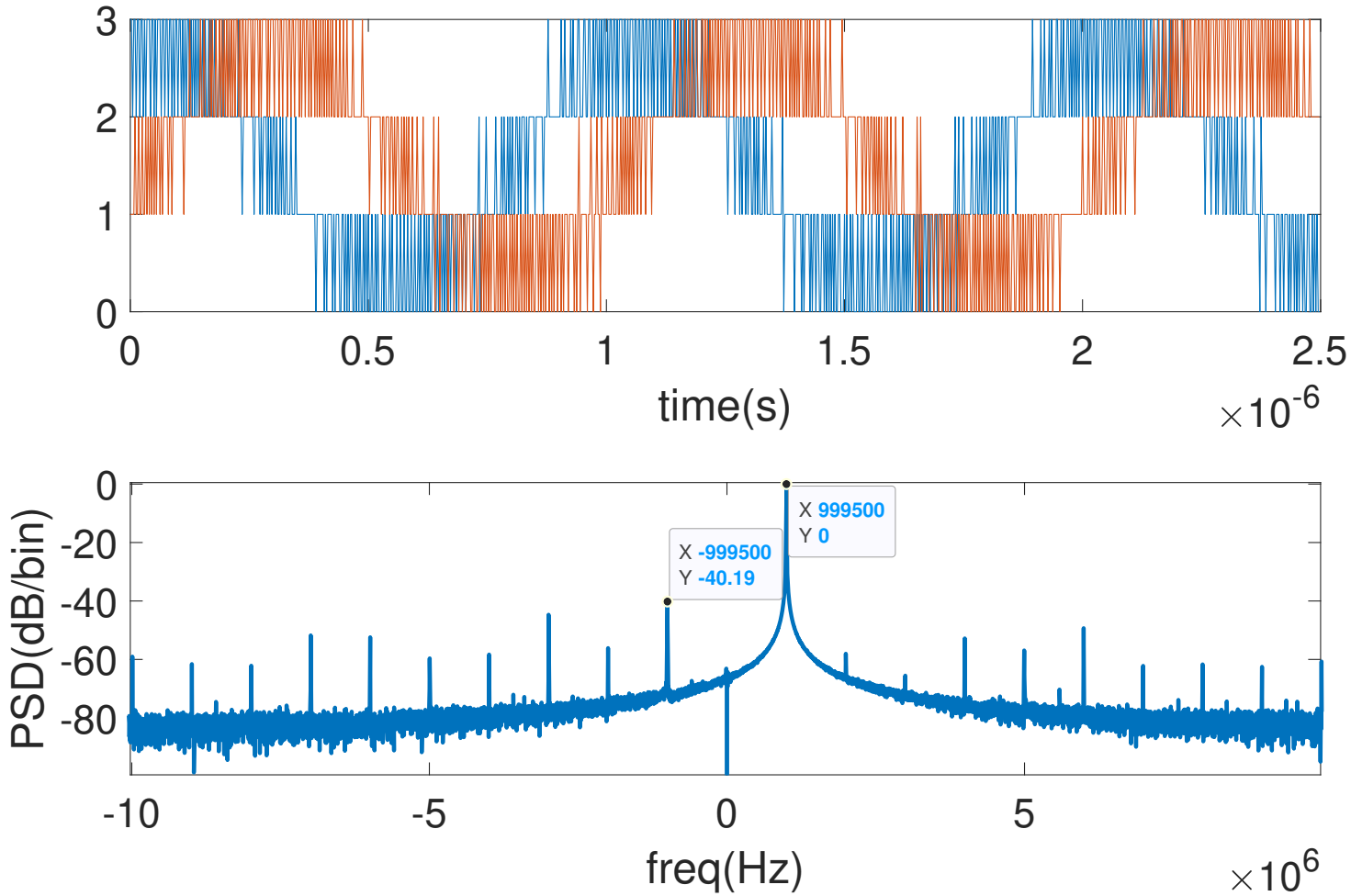


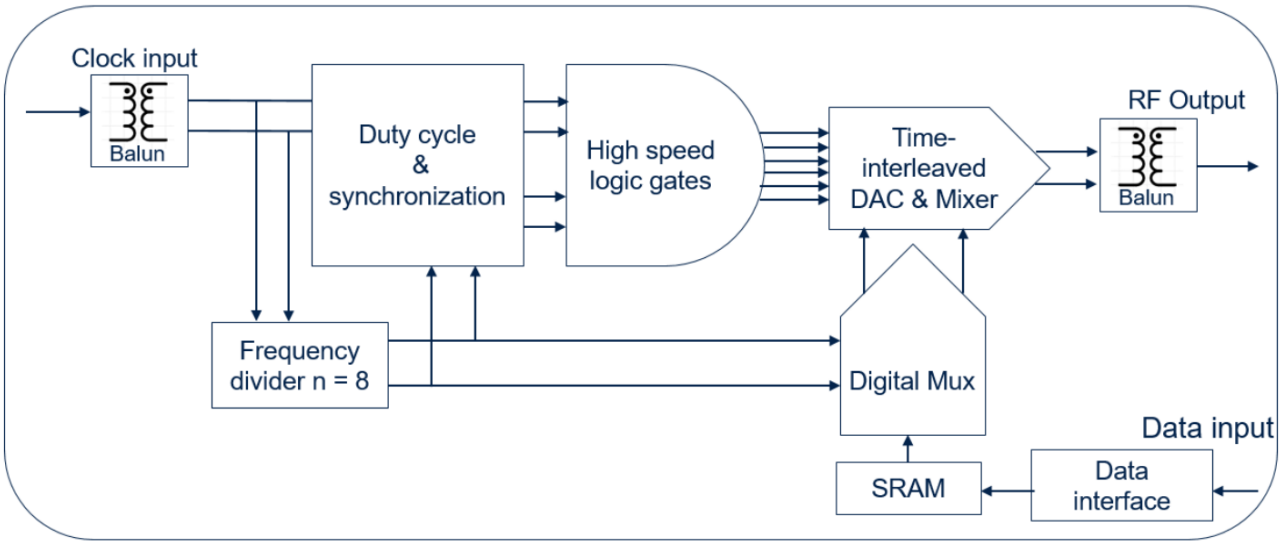
Peak SNDR = 46 dB and 12 dB gain control

Measurements results



I/Q mismatch < -40 dB

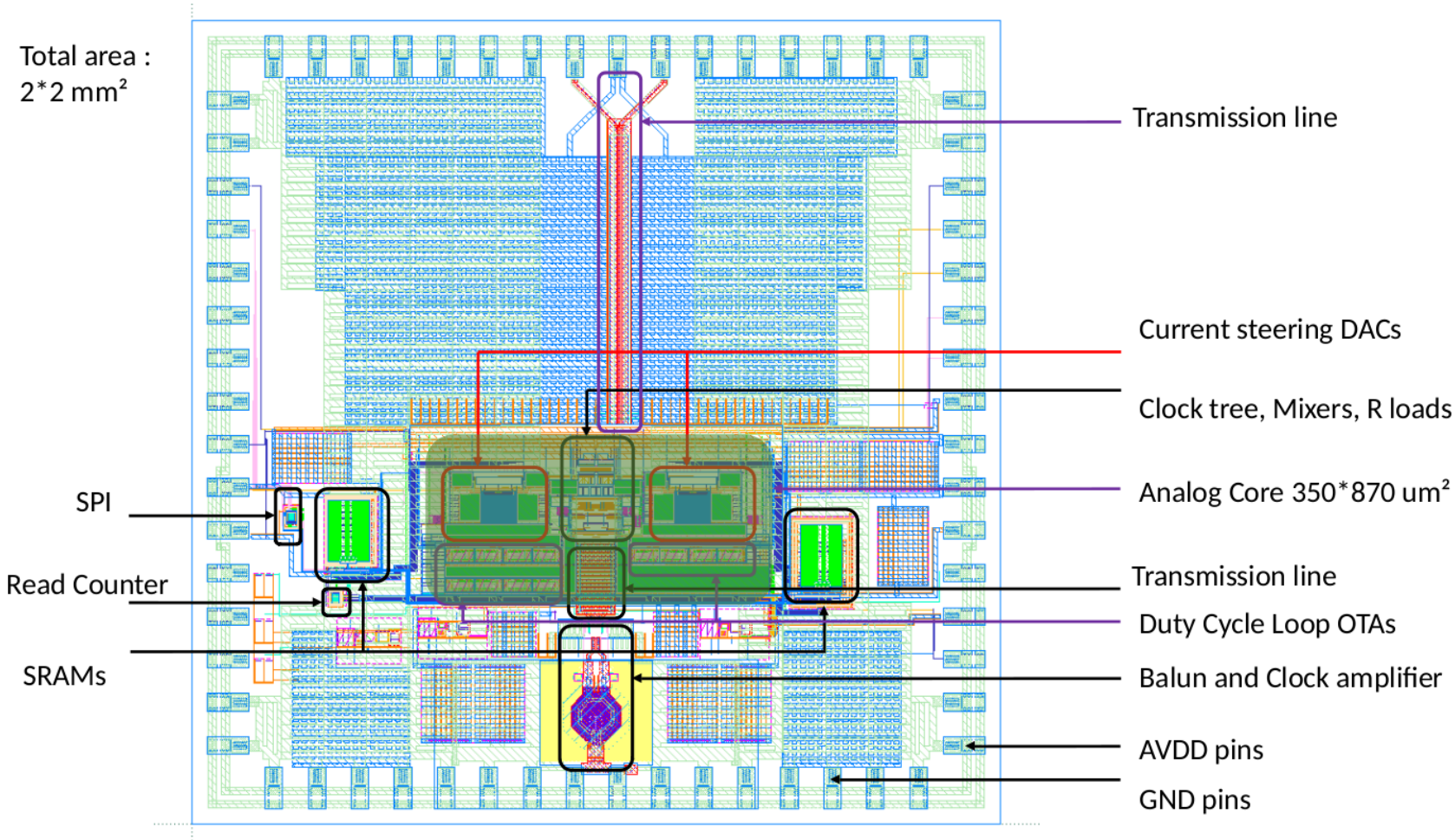
High speed TX for 5G/6G



Process	fs	flo	Nbits	Pout	SFDR	Power Cons.
28 nm	3.5 GS/s	28 GHz	9	-5 dBm	>40 dB	60 mW

- RF Time Interleaved DAC for mmWave applications
- Backgate based calibration of duty cycle

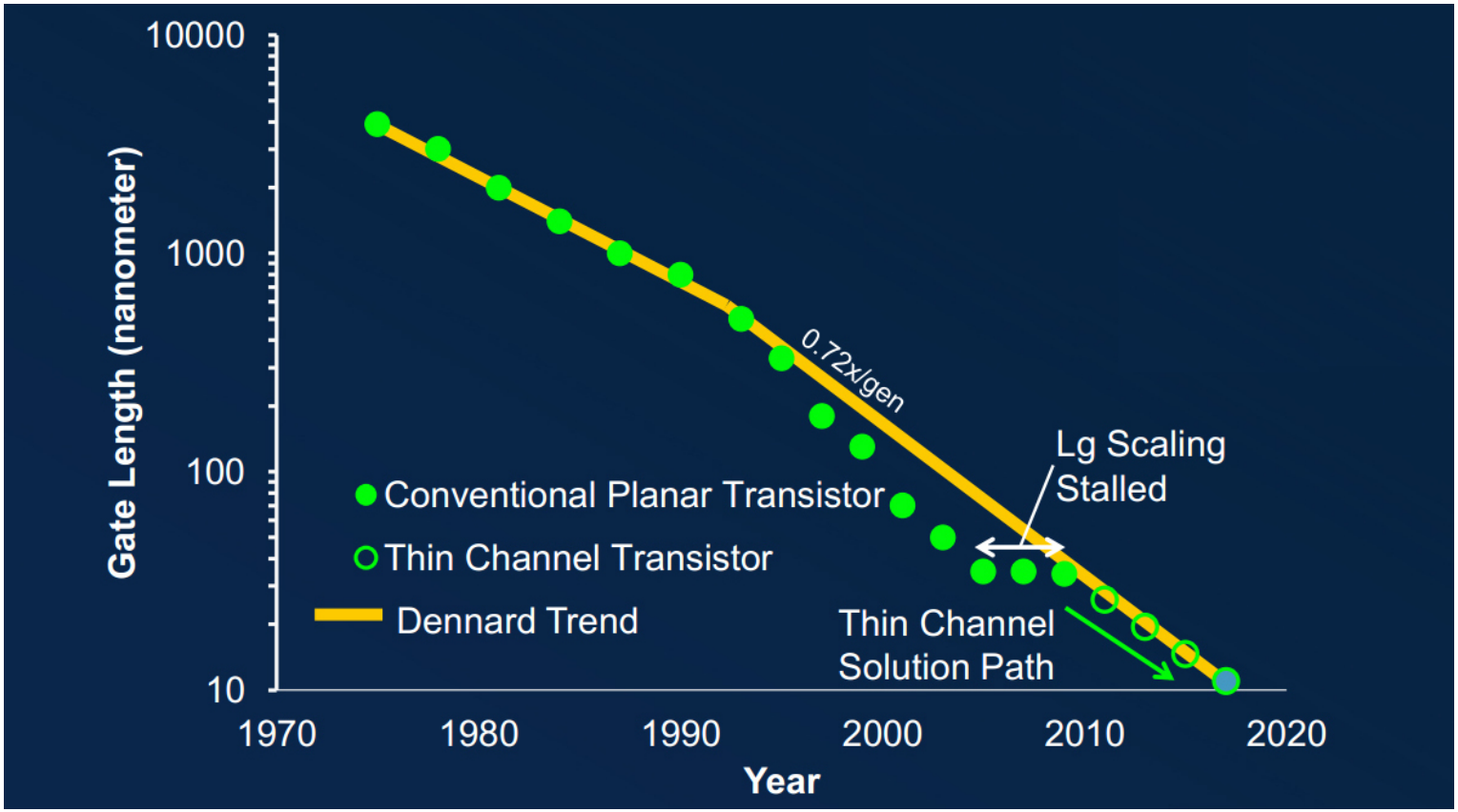
Chip Layout



- The measurements will be done with probes (no package) due to the high frequency
- The chip is waiting for Clement at Lille at IEMN

Outline

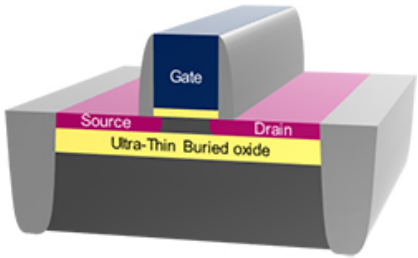
The technology



After 40 nm technology, classical methods of *scaling* have become insufficient

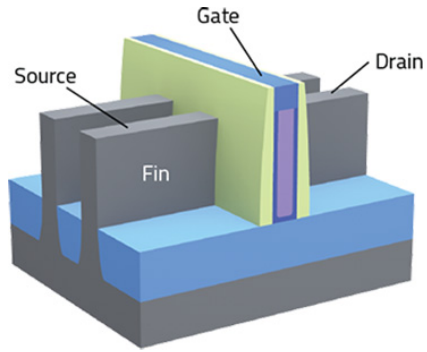
The new families after

Fully Depleted SOI



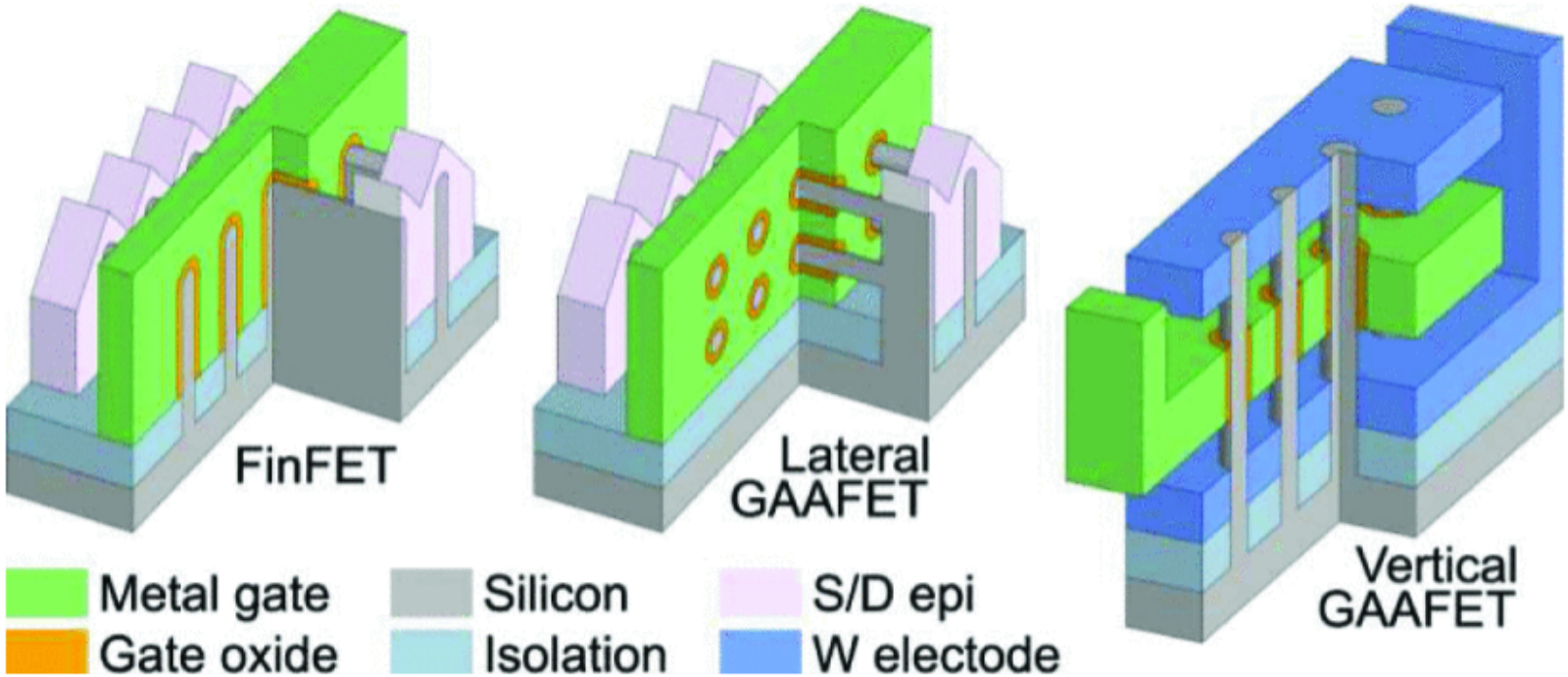
- Planar transistor with a backgate
- Cheaper but seems to be limited to 18 nm or 14 nm
- STM, GF, Samsung

FinFet(Finger Fet)



- 3D finger transistors
- More expensive but shrinkable to at least 7 nm
- Intel, TSMC, Samsung

Sub 7 nm Technologies



- The technology node is not anymore referring to channel length but to the equivalent density
- The transistors are becoming more and more complex and therefore more expensive to produce

Lithography machines

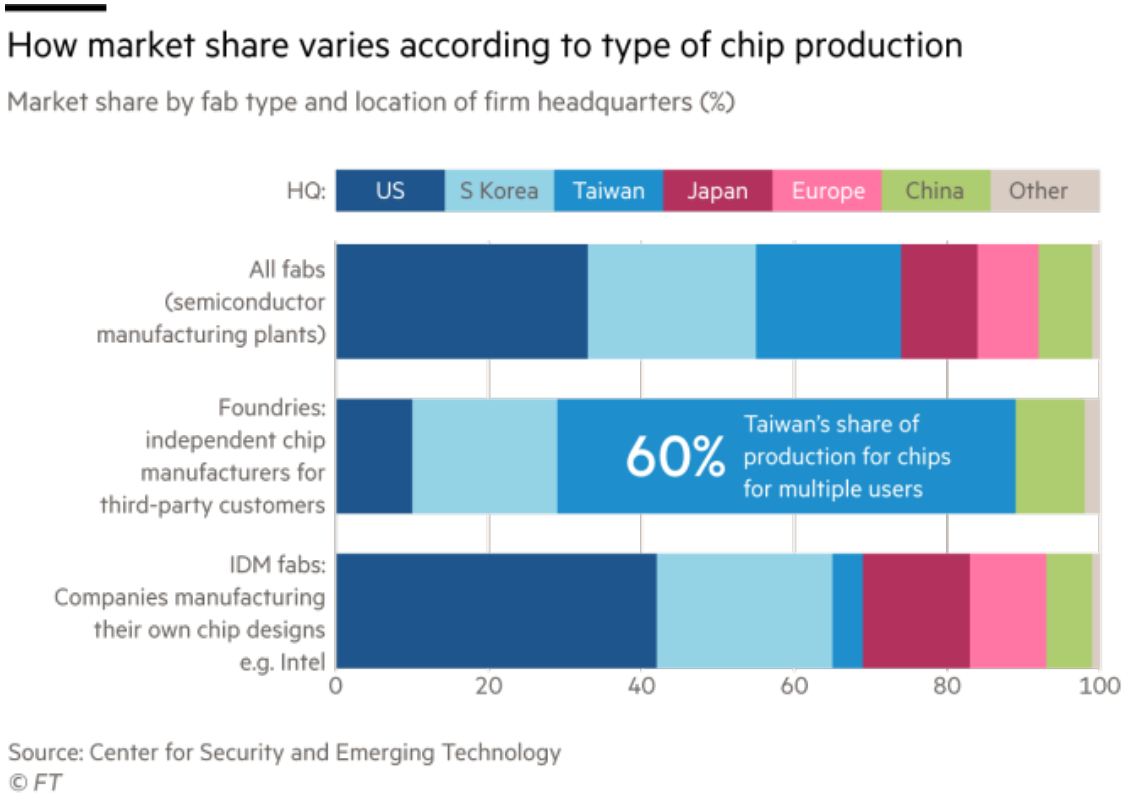
Market share : 50 %

Market share : 38 %

Market share : 12 %

- ASML is the leader of photolithography Equipment, it is dutch company.
- They are also the only producer for latest technology nodes.
  - In 2011 : ASML produced and sold 220 photo-lithography machines.
  - In 2021 : 42 EUV machines (at the modest price of 150 million dollars per machine).
  - The machine weight 180 tons, and requires 18 months to be assembled !

Foundries



- An *Integrated device manufacturer* is a company that both designs and manufactures (Intel, STM)
- A *Fabless Supplier* is a design-only company that outsources manufacturing (Qualcomm)
- A *Pure Play* is a company that only manufactures (TSMC)

Taiwan

US Military Journal

Be ready to destroy TSMC To Deter Chinese Invasion Plan

Outline

Conclusion

- IC design is fun but it is also complex, long and expensive
- COVID, the scaling difficulties, the Taiwan situation are causing the IC shortage but the semiconductor marker is still growing with 640 billion dollars in 2022 (+7%)
- Compared to analog ICs, digital ICs
  - are much easier to design
  - profit much butter from the technology scaling
  - founders optimise their silicon technologies for digital
  - but real world is analog, continuous in time and in amplitude and therefore we need analog ICs

Conclusion

WTF!! You are wrong all the aspects !! (ba dum tsh)

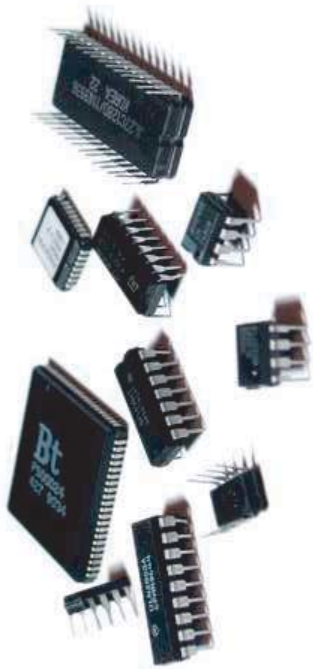
Conclusion

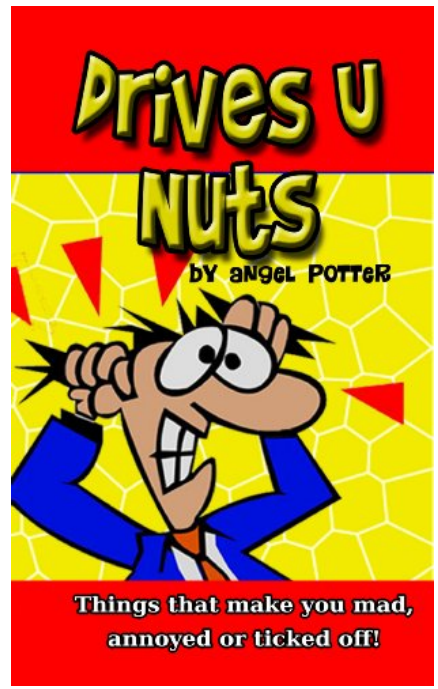
- IC design is fun
- IC design is complex and long
- Compared to analog ICs, digital ICs
  - are much easier to design
  - profit much butter from the technology scaling
  - founders optimise their silicon technologies for digital
  - but real world can be modeled in certain conditions as continuous in time and in amplitude and therefore we need analog ICs

Explaining the title joke

Explaining the title joke

Explaining the title joke





This this the end

Merci pour votre attention

Questions ?

Acknowledgments

Hussein Fakhoury - Main designer for the $\Delta\Sigma$ Data converter
Minh Tien Nguyen - Main designer for the RF receiver
Clement Beauquier - Main designer for the RF DAC
Yves Mathieu - DK master, who makes u make an IC with a make
Karim Ben Kalaia - For all the PCBs and the white plier
Jean Luc Danger - The word play master

Realized DDSR

The methodology detailed in the previous section was used to design several DDSRs at macro-model level or/and transistor level:

- A 4^{th} order fully active CT DDSR suited for GSM/WCDMA/LTE
- A reconfigurable $2^{nd}/3^{rd}$-order DT DDSR architecture for wide frequency range flexible receivers
- A novel approach for ELD compensation in DDSR and in $\Delta\Sigma$ modulator in general based on comparator sharing
- A new architecture for DDSRs suited for non contiguous channel aggregation with an adapted architecture for N-path filters
- A 0.4-6 GHz 4^{th} order DT DDSR in a 65 nm CMOS process

Problems in existing architectures

Continuous Time DDSRs work with a constant sampling frequency f_s regardless of the LO frequency f_{lo}

- ☺ Oversampling is a freedom degree
- ☺ Only one coefficient set needed for all f_{lo}
- ☹ Quantization noise up mixing
- ☹ 2 independent clocks are needed

Discrete Time DDSRs work with $f_s = f_{lo}$

- ☺ No quantization noise up-mixing problem
- ☺ Simpler clock generation
- ☹ Low OSR for low f_{lo}
- ☹ High speed constraints for high f_{lo}

Performance summary

	Koli-09	Wu-14	Englund15	Liu-16	Subramanian-18	Bui-19*	This Work*
Arch.	4^{th} order CT loop	2^{nd} order DT loop	4^{th} order CT loop	5^{th} order CT loop	4^{th} order CT loop	5^{th} order CT loop	4^{th} order DT loop
Process (nm)	65	65	40	65	65	65	65
LO (GHz)	0.9	0.4-4	0.7-2.7	0.6-3.0	0.5-2.75	0.4-3.6	0.4-6
f_s (MHz)	1000	Equal to LO	1250	592	200	61.44-592	400-425
BW (MHz)	9	10	15	10	10	1.92-18.5	10
IN-IIP3 (dBm)	-12	10	-20	-23	-21	-15	3
NF (dB)	6.2	16	5.9-8.8	2.4-3.5	6.1-10.8	2.5	9.0
Peak SNDR (dB)	56	52-65	40-43	74	36	58.8	62
Power Cons.(mW)	80	17-70.5	90	20	9.3-16.2	25	40.6-62.8

Simulation

Performance summary

	Koli-09	Wu-14	Englund15	Liu-16	Subramanian-18	Bui-19*	This Work
Arch.	4^{th} order CT loop	2^{nd} order DT loop	4^{th} order CT loop	5^{th} order CT loop	4^{th} order CT loop	5^{th} order CT loop	4^{th} order DT loop
Process (nm)	65	65	40	65	65	65	65
LO (GHz)	0.9	0.4-4	0.7-2.7	0.6-3.0	0.5-2.75	0.4-3.6	0.4-0.8
f_s (MHz)	1000	Equal to LO	1250	592	200	61.44-592	350-450
BW (MHz)	9	10	15	10	10	1.92-18.5	10
IN-IIP3 (dBm)	-12	10	-20	-23	-21	-15	2.7
NF (dB)	6.2	16	5.9-8.8	2.4-3.5	6.1-10.8	2.5	25
Peak SNDR (dB)	56	52-65	40-43	74	36	58.8	46
Power Cons.(mW)	80	17-70.5	90	20	9.3-16.2	25	43@400 MHz

Measurement

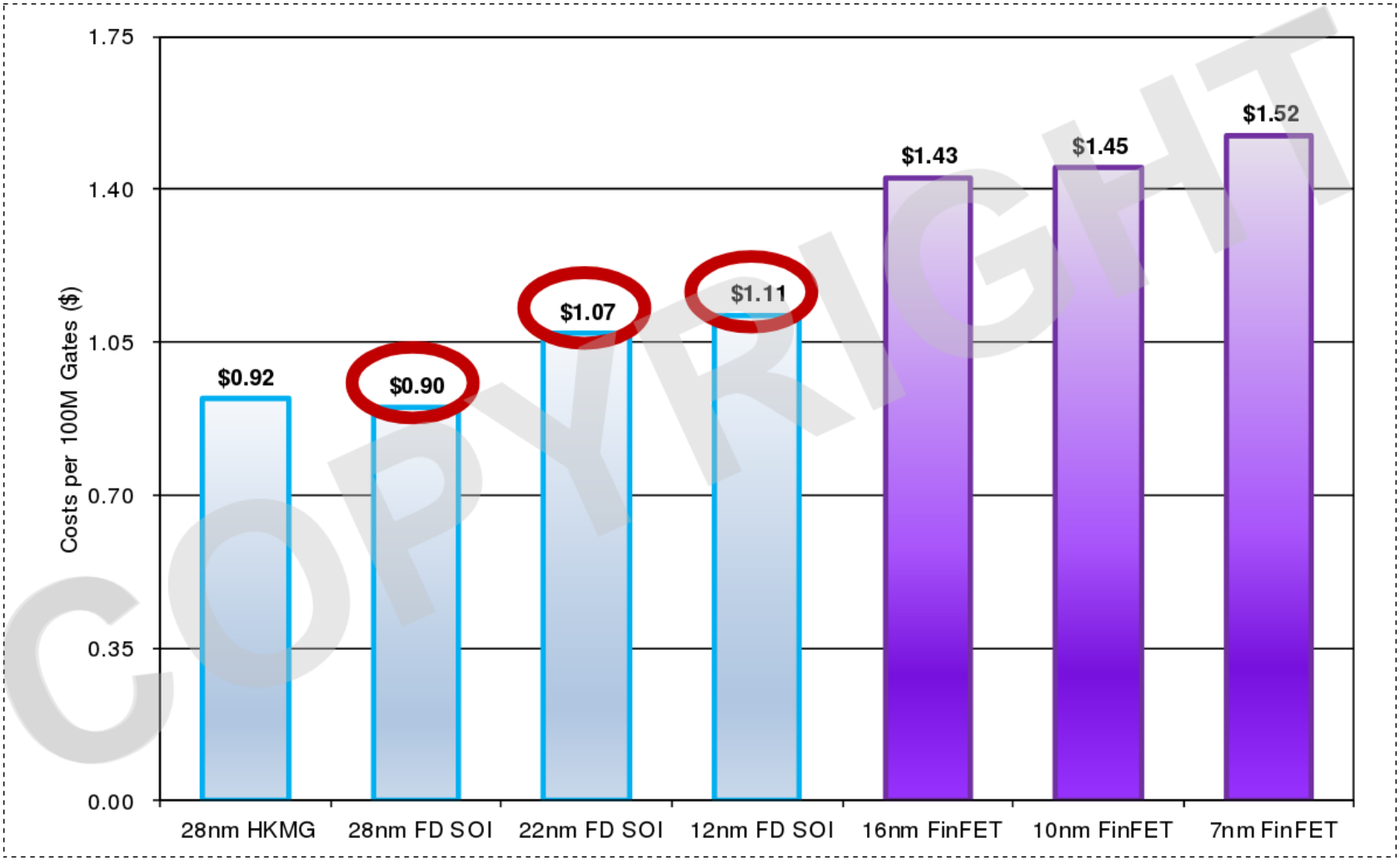
Performance summary

	Koli-09	Wu-14	Englund15	Liu-16	Subramanian-18	Bui-19*	This Work
Arch.	4^{th} order CT loop	2^{nd} order DT loop	4^{th} order CT loop	5^{th} order CT loop	4^{th} order CT loop	5^{th} order CT loop	4^{th} order DT loop
Process (nm)	65	65	40	65	65	65	65
LO (GHz)	0.9	0.4-4	0.7-2.7	0.6-3.0	0.5-2.75	0.4-3.6	0.4-0.8
f_s (MHz)	1000	Equal to LO	1250	592	200	61.44-592	350-450
BW (MHz)	9	10	15	10	10	1.92-18.5	10
IN-IIP3 (dBm)	-12	10	-20	-23	-21	-15	2.7
NF (dB)	6.2	16	5.9-8.8	2.4-3.5	6.1-10.8	2.5	25
Peak SNDR (dB)	56	52-65	40-43	74	36	58.8	46
Power Cons.(mW)	80	17-70.5	90	20	9.3-16.2	25	43@400 MHz

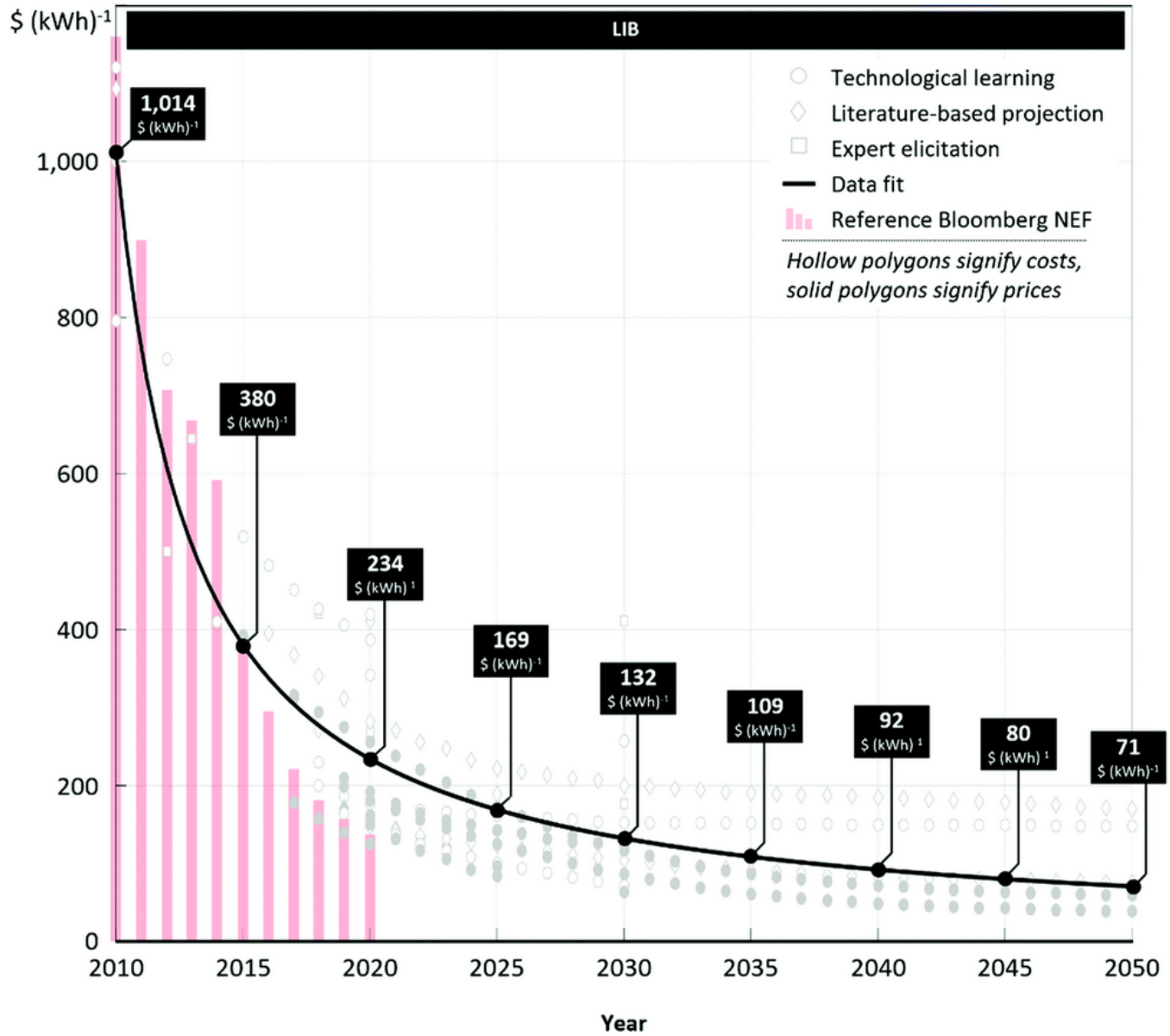
Measurement

- Investigations are ongoing to understand the performance difference
- For higher frequencies $f_{lo} > 1.2$ GHz, a second PCB will be fabricated

Context



Context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Literature-based projection
Expert elicitation
Data fit
Reference Bloomberg NEF
Hollow polygons signify costs,
solid polygons signify prices
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$ (kWh)-1
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$ (kWh)-1
234
$ (kWh)-1
169
$ (kWh)-1
132
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109
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92
$ (kWh)-1
80
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71
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600
400
200
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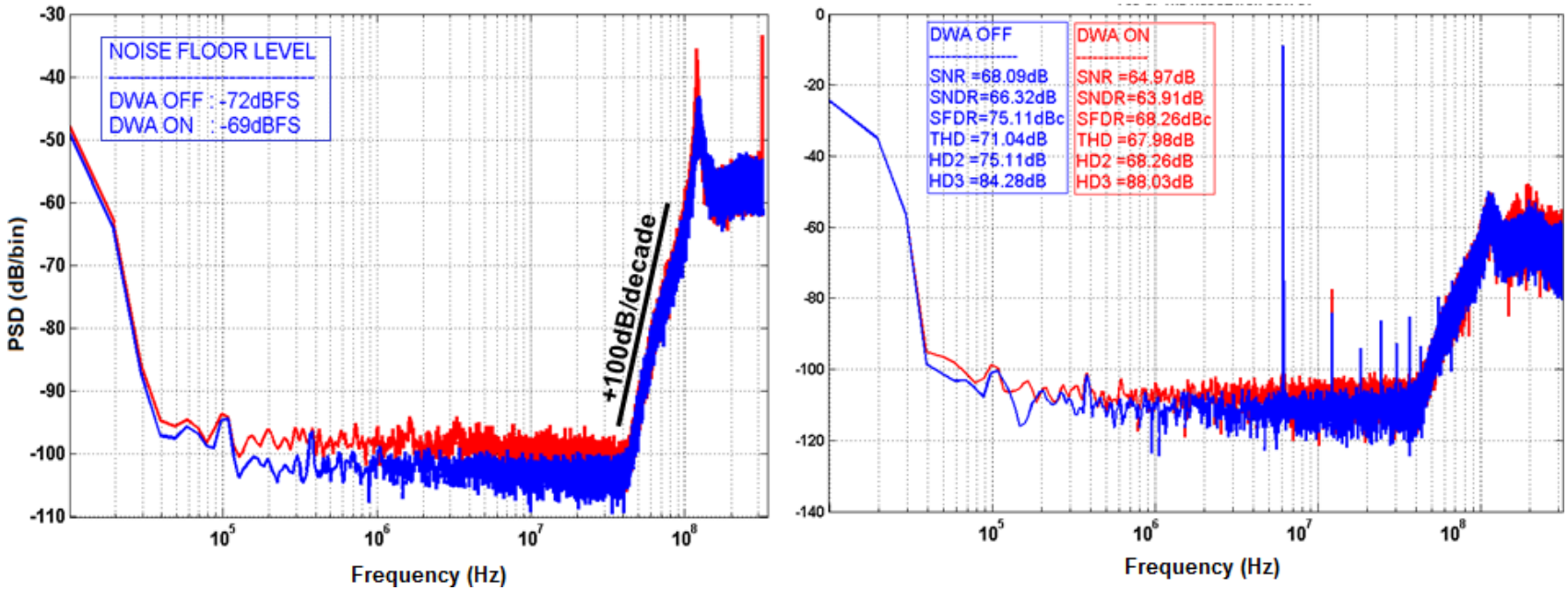
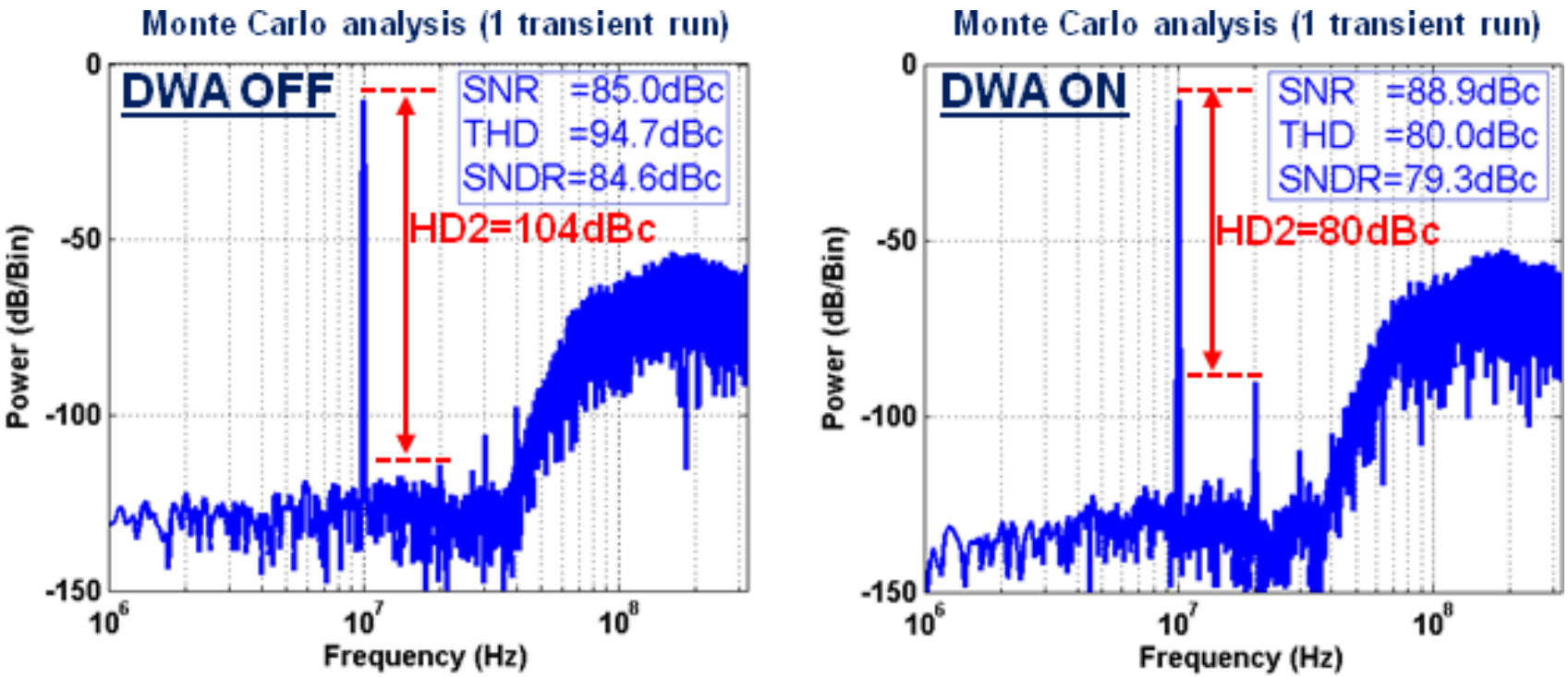
2010
2015
2020
2025
2030
2035
2040
2045
2050
Year

DWA measurement problem



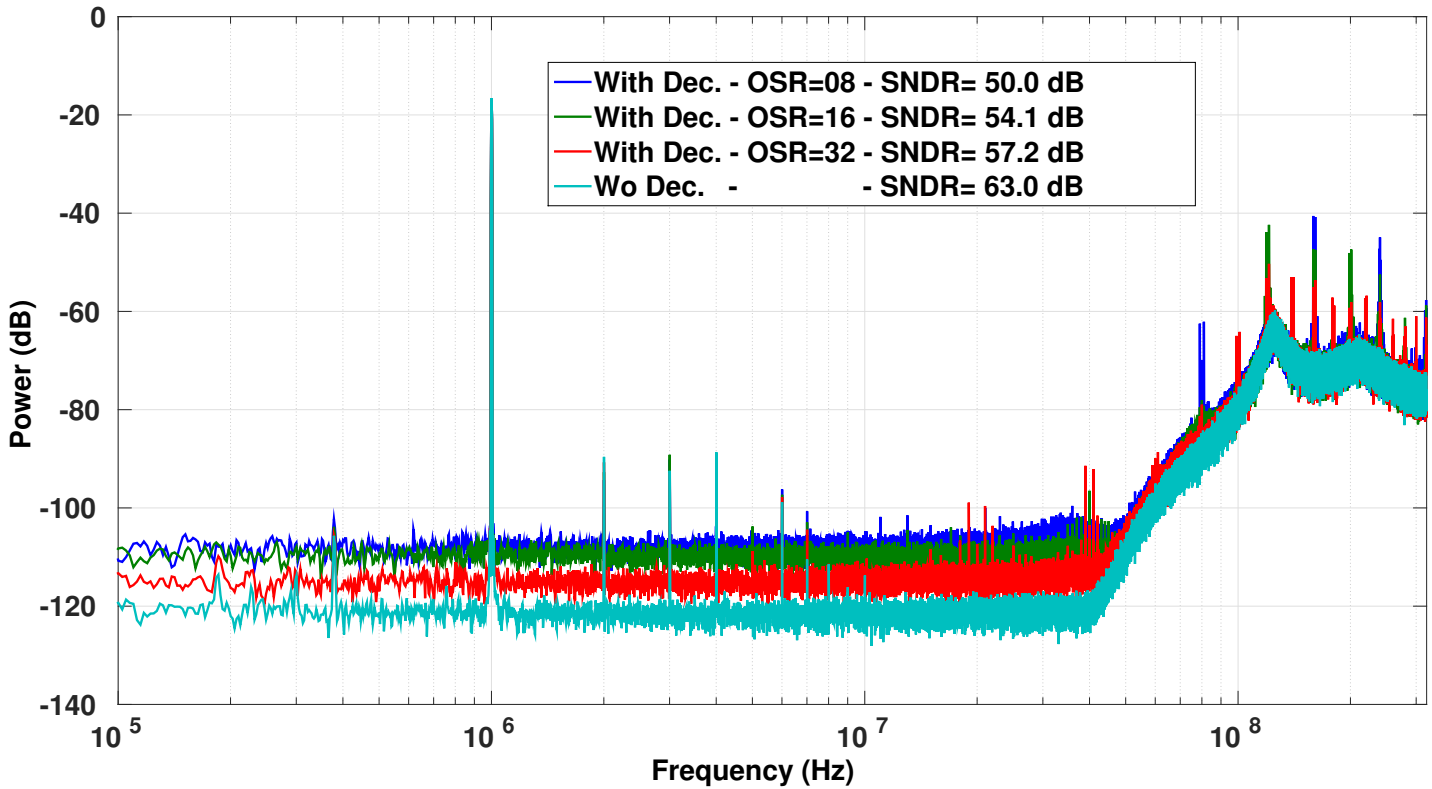
PSD of the $\Delta\Sigma$ modulator output (65536 FFT points) (b) Measured SNR and SNDR as a function of the input signal level (finput=6 MHz)

DWA measurement problem analysis

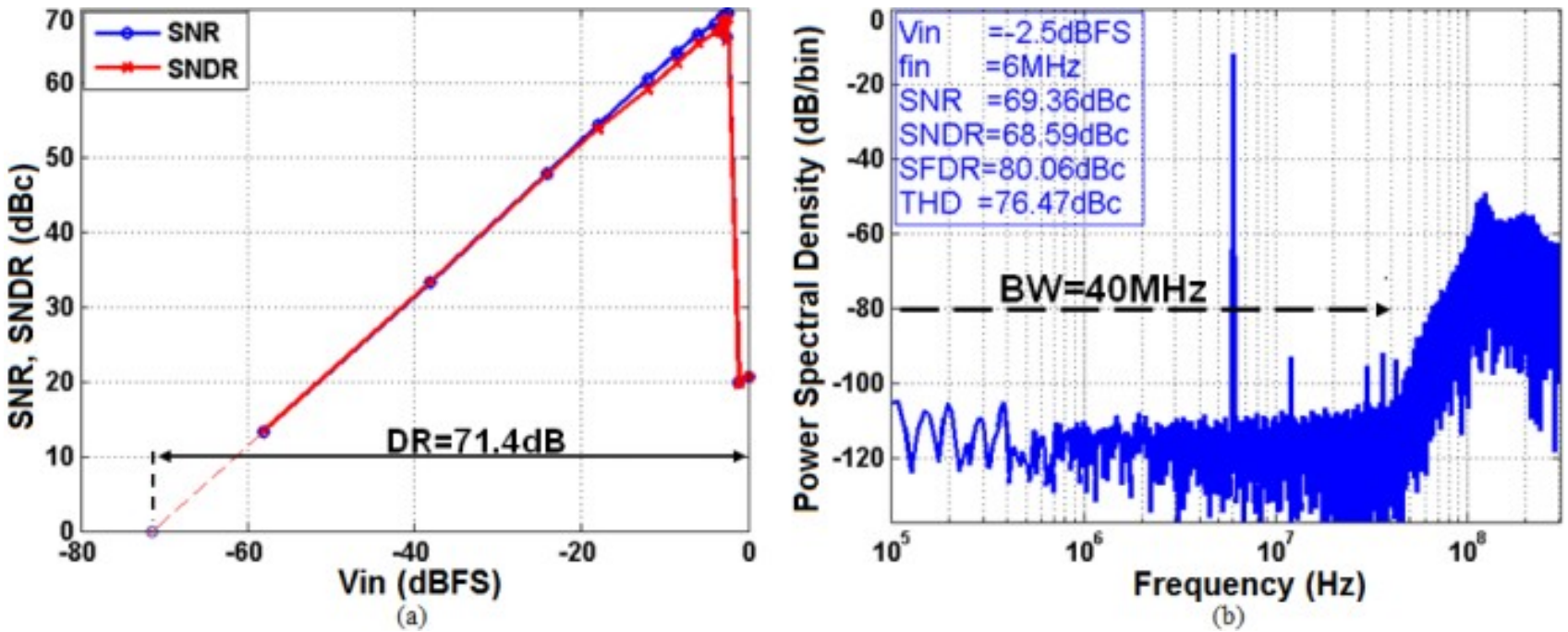


PSD of the $\Delta\Sigma$ modulator output (65536 FFT points) (b) Measured SNR and SNDR as a function of the input signal level (finput=6 MHz)

Decimator measurement problem

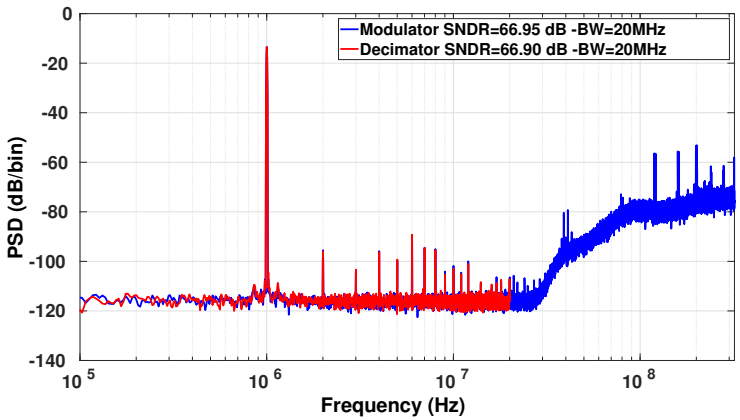


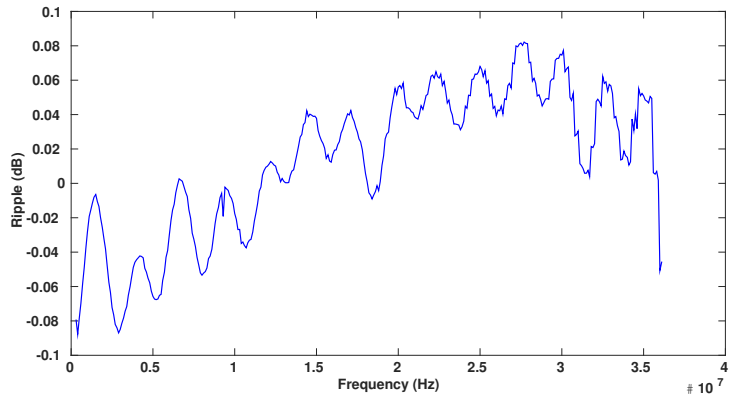
Measurements - Modulator



Left) PSD of the $\Delta\Sigma$ modulator output (65536 FFT points)
Right) Measured SNR and SNDR as a function of the input signal level (finput=6 MHz)

Measurements - Decimator





Left) Spectums of the modulator and decimator outputs for an OSR of 16 Right) Frequency response of the decimation filter