Picosecond timing in High Energy Physics

Christophe de LA TAILLE (OMEGA)

Organization for Micro-Electronics desiGn and Applications

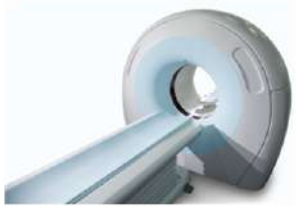
OMEGA microelectronics Laboratory

- National Micro-electronics design center to address readout ASICs needed for instrumentation in Particle Physics.
- 12 CNRS staff engineers, highly specialized in low noise, rad-hard, high speed mixed-signal readout ASICs
- Location at Ecole Polytechnique provides strong links with teaching and industrial partners in Advanced Technologies
- Technology transfer with WEEROC startup

Research, Institute

Industry, company

Education, School



OMEGA ASICs : overview

SKIROC

SPIROC

MICROROC

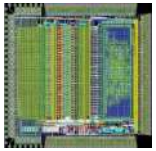
MAROC3

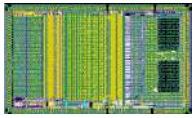
2006

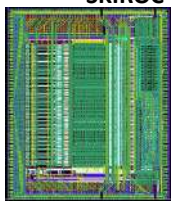
PETIROC

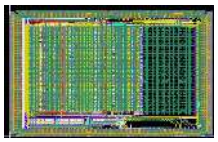
SPACIROC

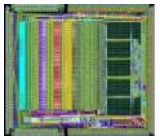
HARDROC







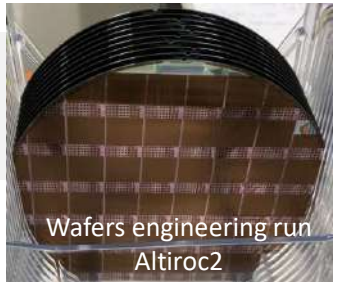




9 engineering runs in 9 years :

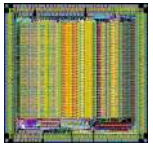
AMS SiGe 0,35um 2014, 2016, 2018

TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)



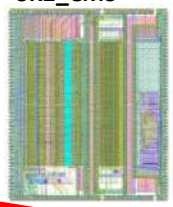
TRIROC

CITIROC

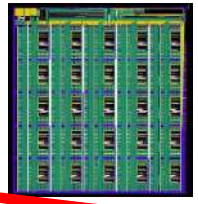


CATIROC

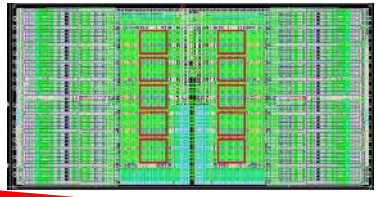
SK2_CMS



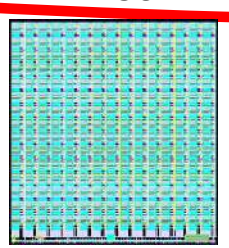
ALTIROC1



HGCROC

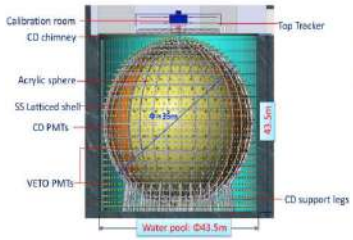


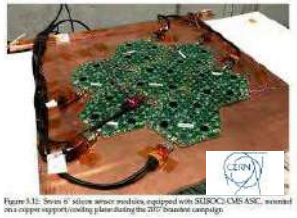
ALTIROC2



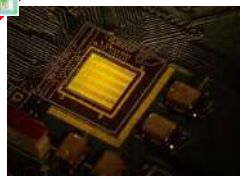
HKROC

2023



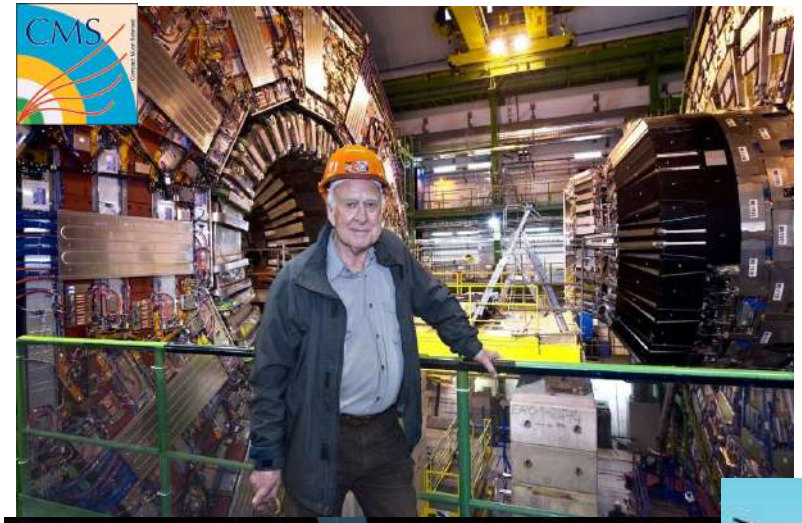


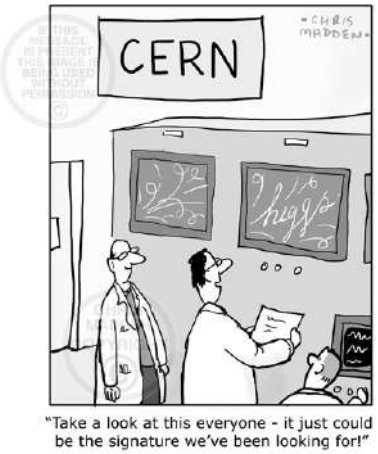
ICE semina

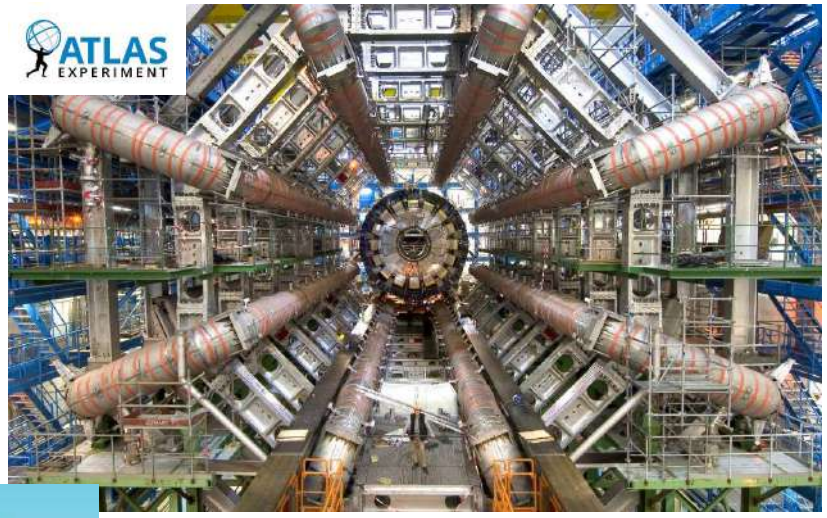


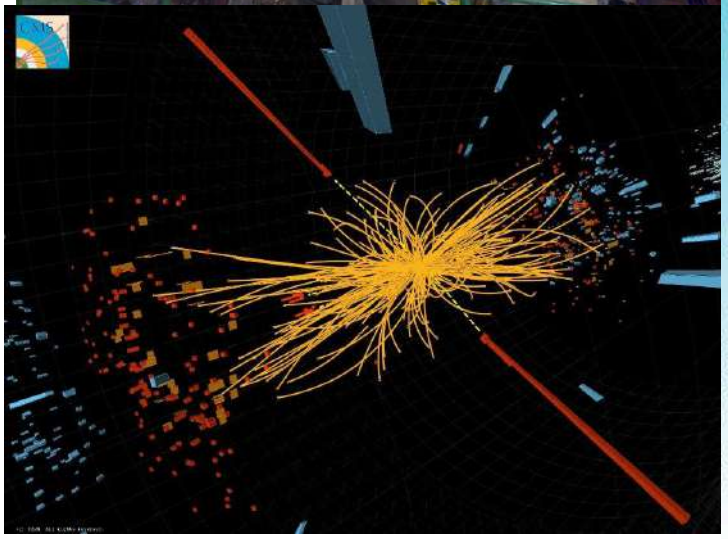
Electronics in HEP experiments

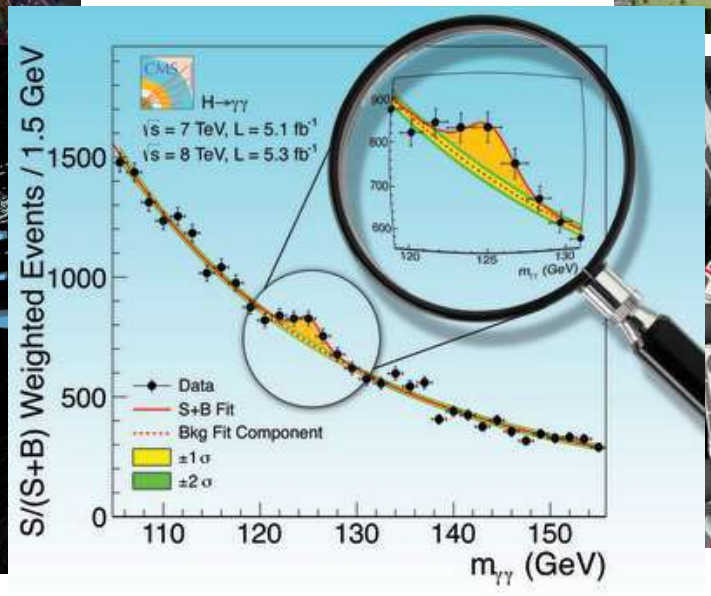
- A lot of electronics in the experiments…which impacts the detectors' performance

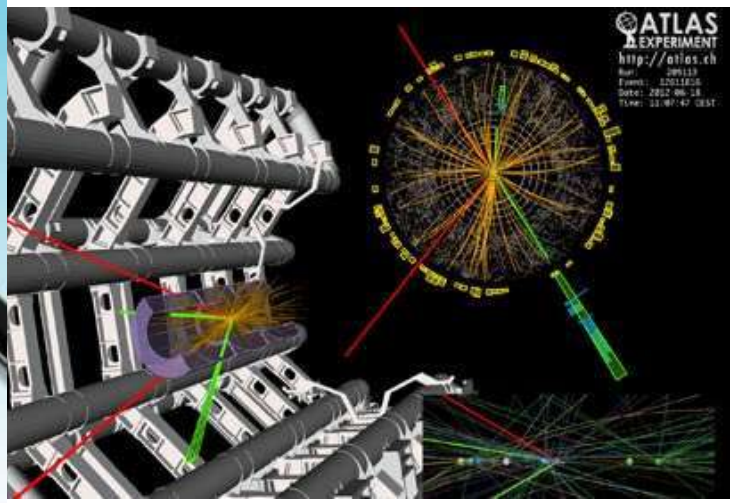








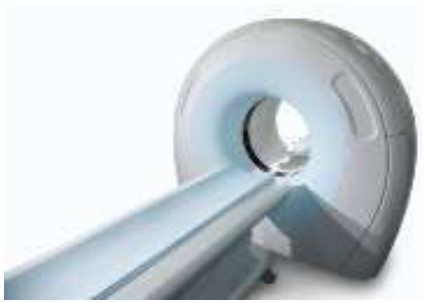




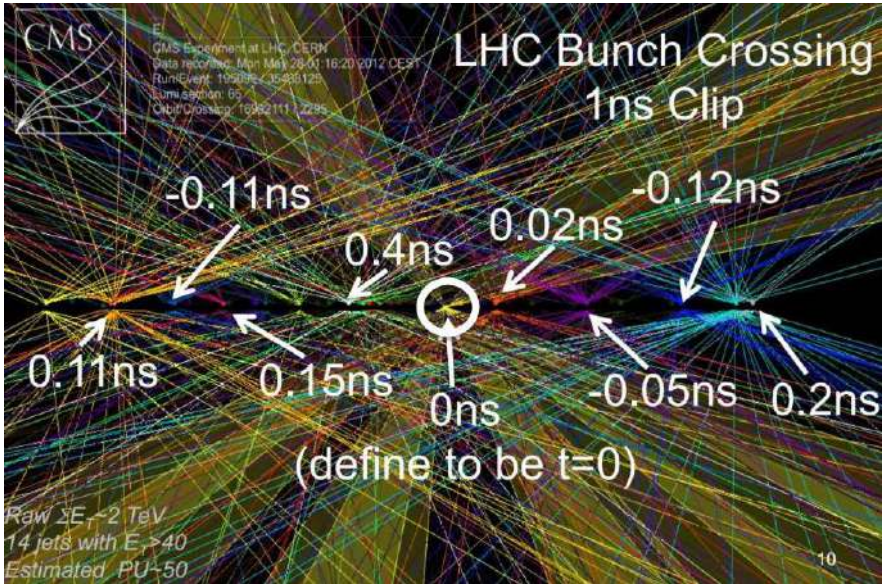
Need for timing

- Time resolution <50ps required by many experiments/applications keeping low power, large dynamic range ….

- **PET/ Time of Flight** measurements
  - SiPMs, lots of light
  - Time resolution <100ps



- **« 5D Calorimetry » CMS HGCAL**
  - Si PIN diodes : no gain.
  - . Timing ability ~50ps (for > 10 mips desirable)



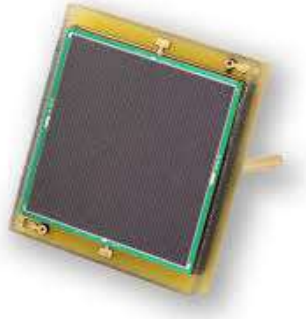
- **Pileup rejuection : MIP timing detectors (ATLAS & CMS)**
  - LGAD sensors : Time performance ~30 ps : To reject Time Pile up events => better particle identification

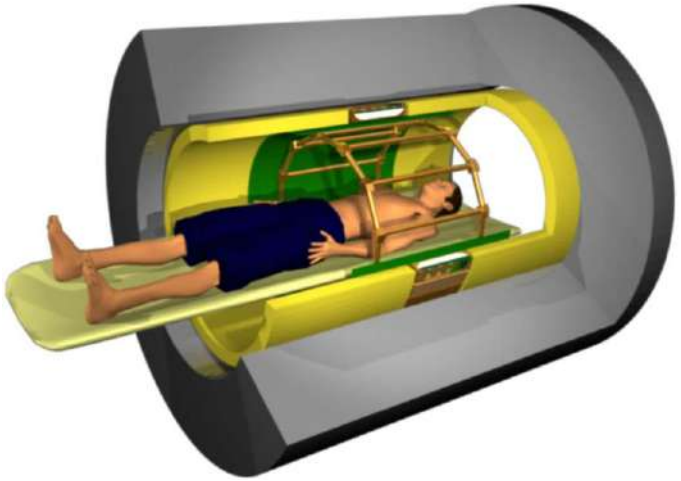
- **TOF detectors/ PID** (SiPM)
  - MCPs, SiPMs… Few photoelectrons.
  - Time performance ~30 ps

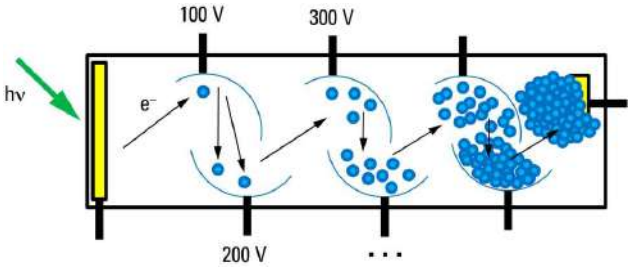
- …

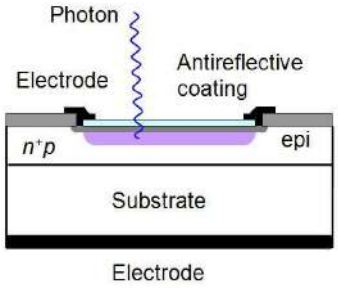
Single photon sensors & timing information

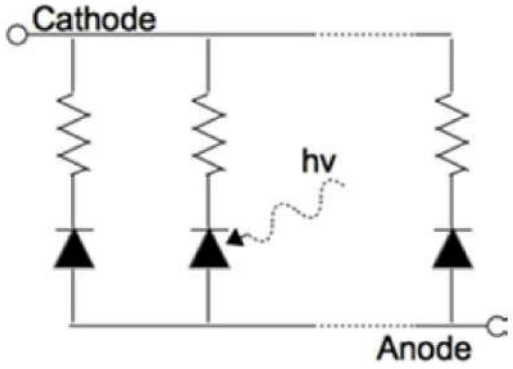
- Photomultipliers, silicon photomultipliers

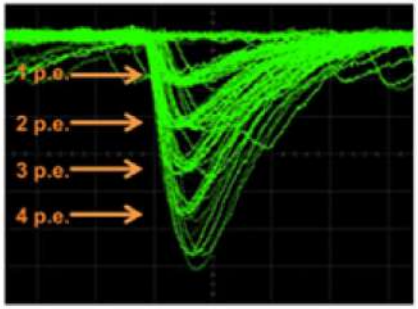


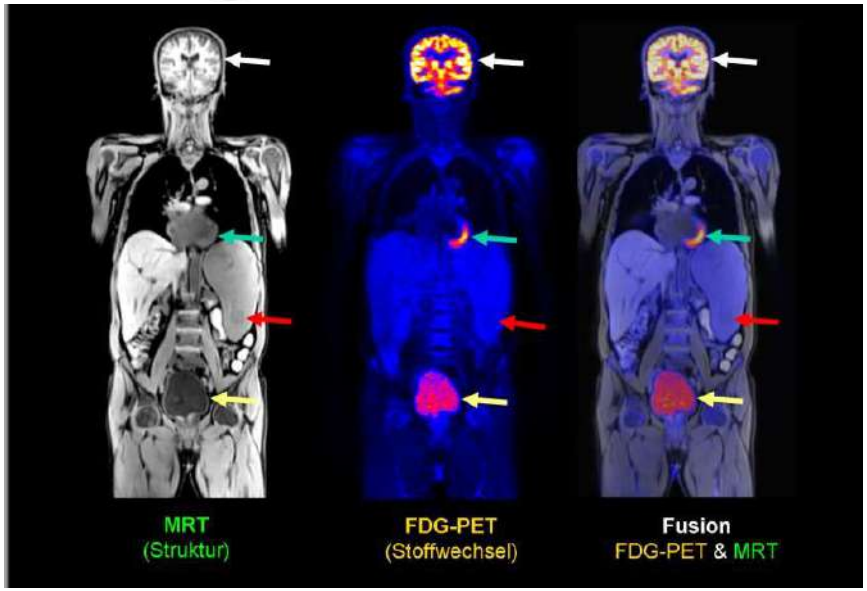












TOF-PET imaging

[G. Terragni et al. IEEE/NSS-MIC conf Tampa 2024]

TOF-PET

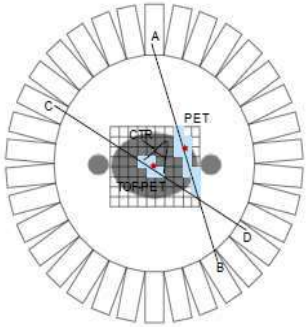
Fundamental requirements

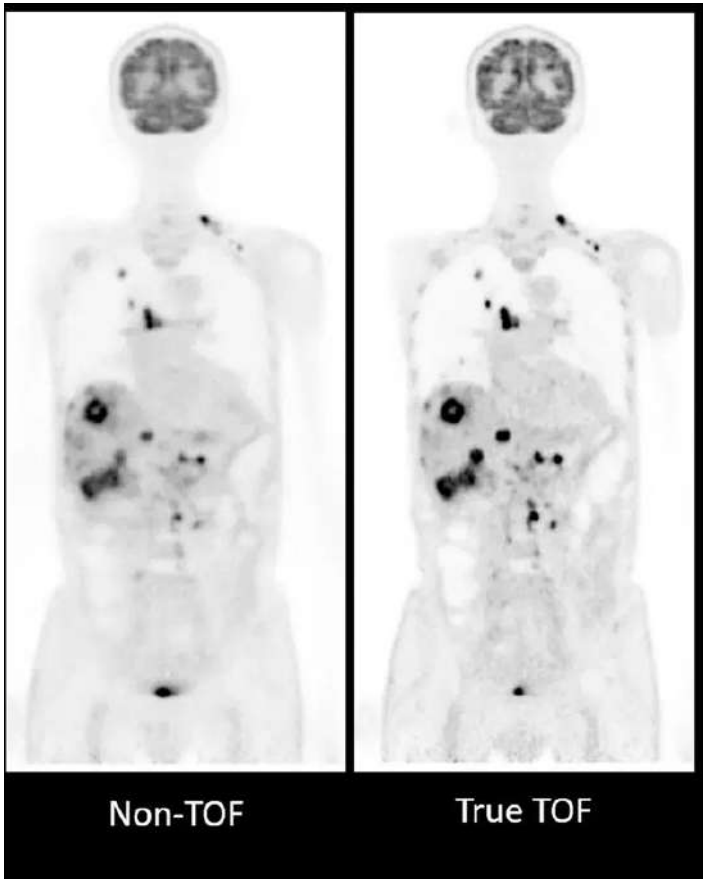
To obtain as many counts as possible:

- High **sensitivity** → **Long scintillator** maximize sensitivity
  But
  Parallax effect degrades the spatial resolution

To characterize them as accurate as possible:

- High **spatial resolution** → **Segmentation** improves spatial resolution
  And
  Recovering resolution is possible if the **depth of interaction (DOI)** of the gamma rays is measured
- High **timing resolution** → Improve **event localization** along the line of response (LOR)
  And
  Improve **signal-to-noise ratio** (SNR)
- High **energy resolution**





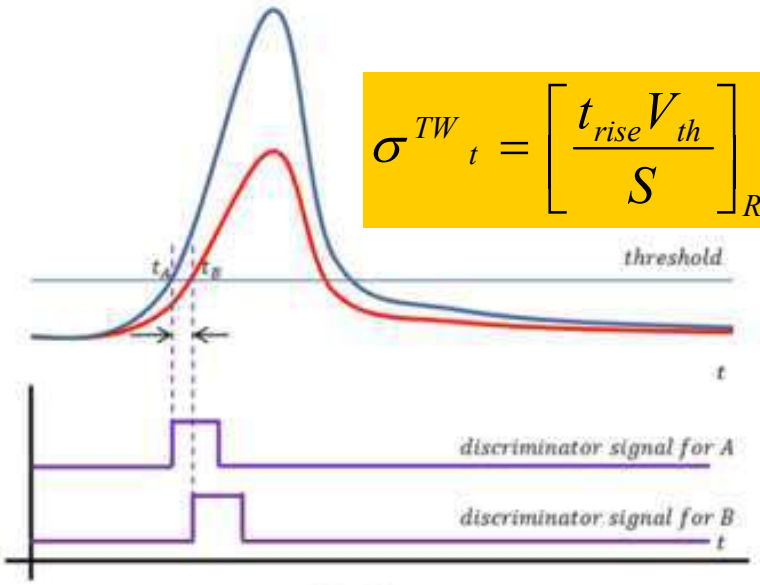
Time walk and time jitter

[N. Cartiglia et al. https://indico.cern.ch/event/485239/overview]

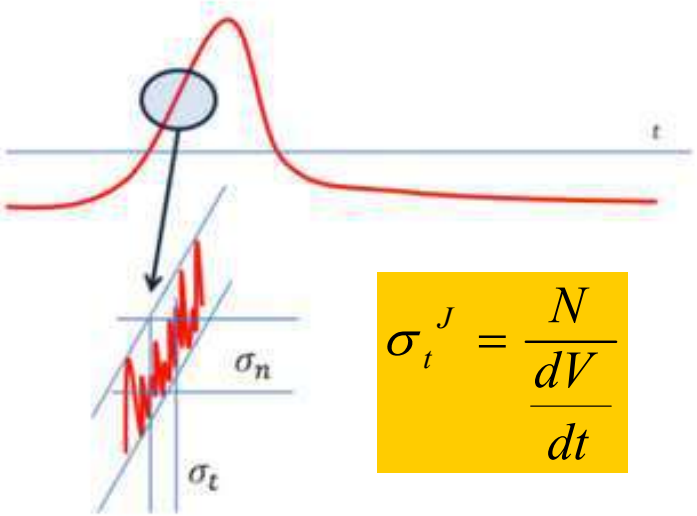
Jitter: the noise is summed to the signal, causing amplitude variations

Time walk: the voltage value Vo is reached at different time for signal of different amplitudes

$$\sigma^{TW}{}_t = \left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}$$



Time walk effect



$$\sigma_t^{J} = \frac{N}{\frac{dV}{dt}}$$

Jitter effect

Due to the physics of signal formation

Mostly due to electronic noise

$$\sigma_t^{2} = \left(\frac{t_{rise}}{S/N}\right)^2 + \left(\left[\frac{t_{rise} V_{th}}{S}\right]_{RMS}\right)^2 + \left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2$$

Jitter

Time Walk

TDC

Timing optimization : common view

- Jitter due to electronics noise:

$$\sigma_t^{\,J} = \frac{N}{\frac{dV}{dt}}$$

- also presented as j = tr / (S/N)
- dV/dt prop to BW, N prop to √ BW => jitter prop to 1/√BW

⇒ « the faster the amplifier the better the jitter ? »

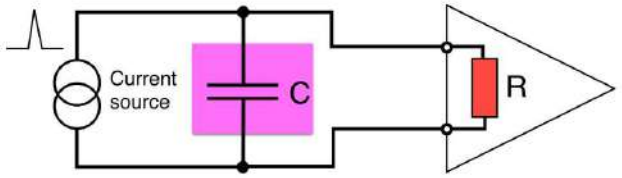
⇒ « High speed preamps need to be low impedance (50 Ω or less) »

NB : tr = $t_{10\text{-}90\%}$ = 2.2 tau.

f_{-3dB} = 1/2πtau = 0. 35 / $t_{10\text{-}90\%}$

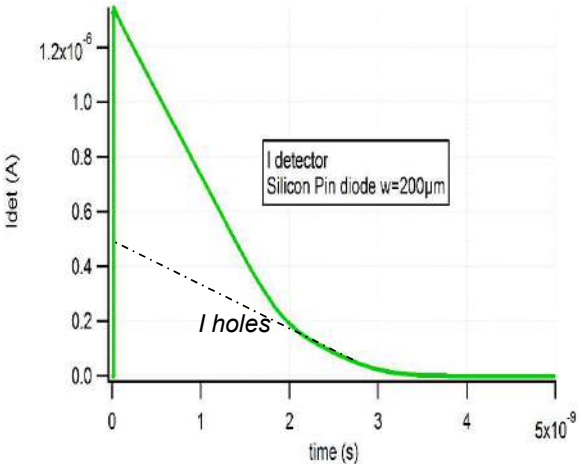
f_{-3dB} = 1 GHz <-> $t_{10\text{-}90\%}$ = 300 ps

1 ps = 300 µm in vacuum

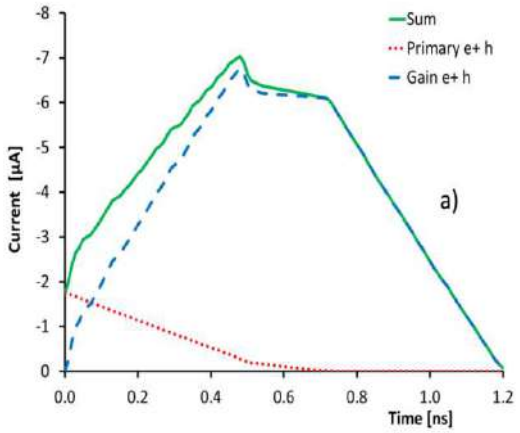


Signal : detector current

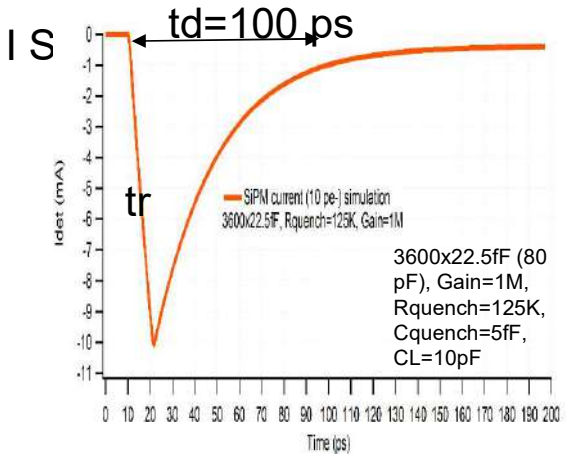
- PN diode w =200µm
- Very short rise time : tr~10ps
- Relatively long «drift time» : td~2ns



- LGAD sensor w =50µm
- rise time : tr~500ps
- Decay time» : td~700ps



- SiPM detector (10pe-)
- very short rise time : tr~10 ps
- Short duration : td~100ps),

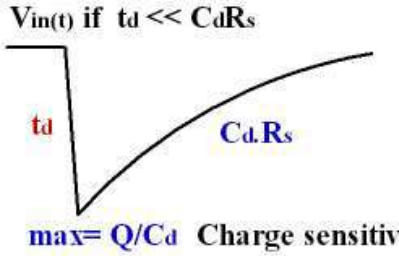


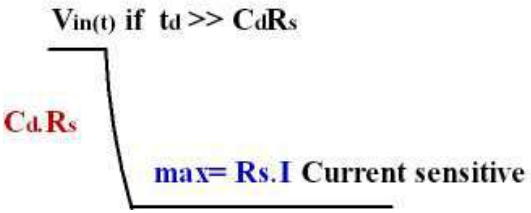
Sensor people : ***"the beautiful risetime of the detector is spoilt by the electronics"***

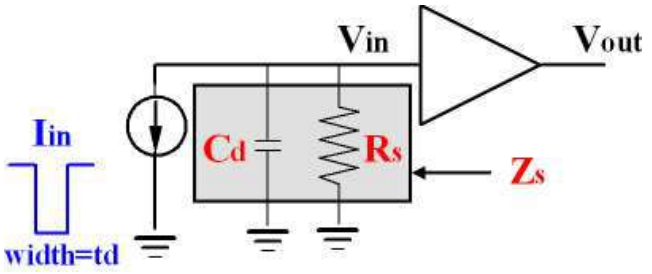
Detector impedance and input voltage

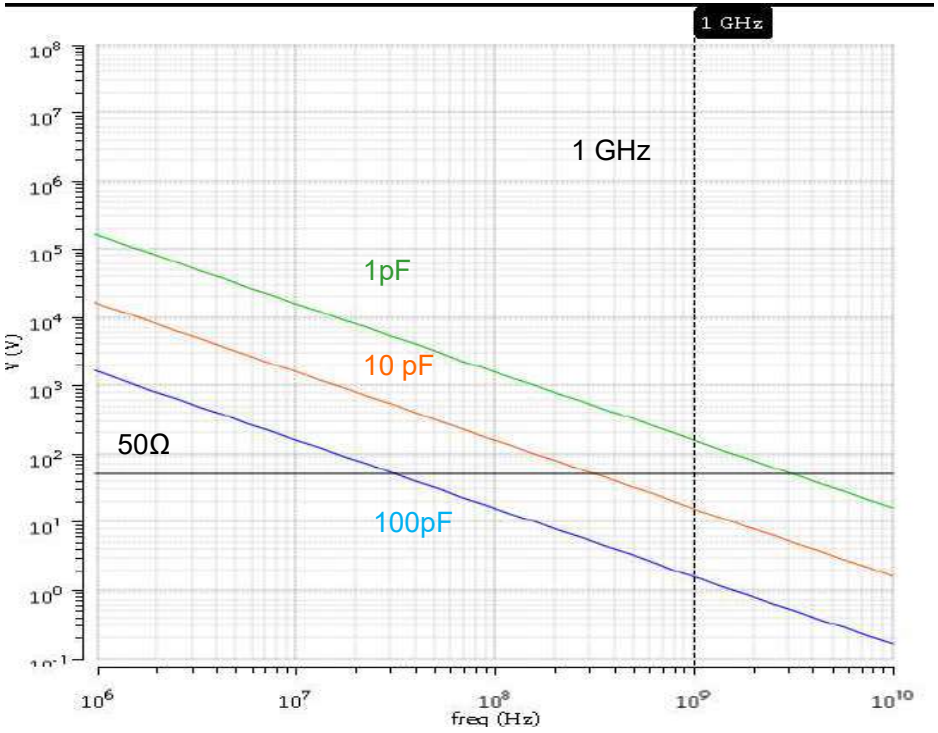
- 1 GHz, Cd=few tens of pF, input signal width <1ns
- Cd>1 pF, Zs@1GHz dominated by Cd
- Rise time: tr= td when td<< $R_S C_d$ and tr= $R_S C_d$ when td>> $R_S C_d$

At HF : difficult to beat the capacitance => signal integrated on Cd



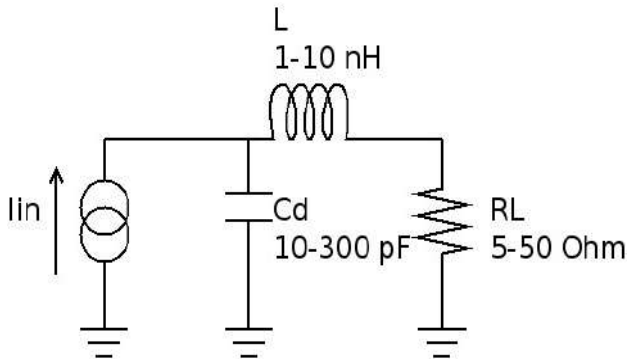


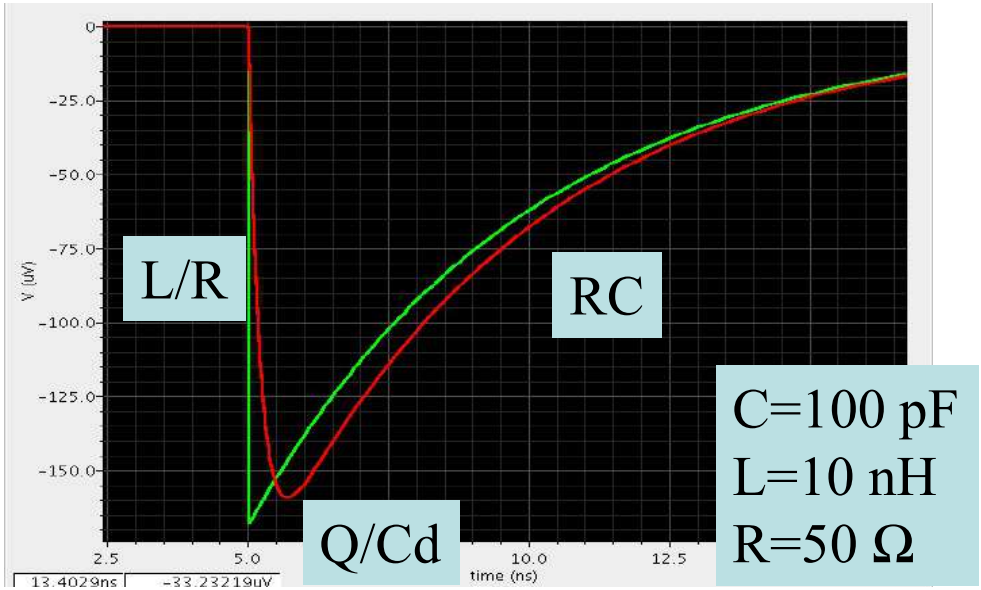


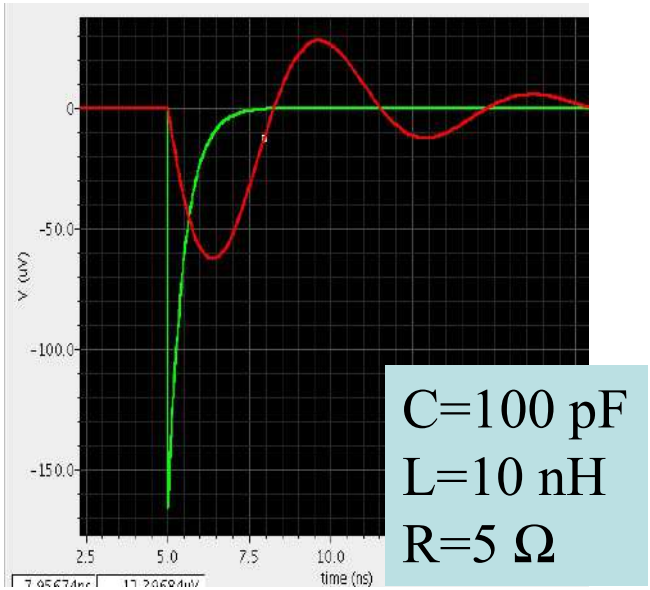


Examples of pulse shapes

- SiPM pulse : Q=160 fC, Cd=100 pF, L=0-10 nH, R_{PA}=5-50 Ω
- Sensitivity to parasitic inductance
- Choice of R_{PA} : decay time, stability
- Small R_{PA} not necessarily the fastest
- Convolve with current shape… (here delta)







Jitter optimization

- Jitter is given by [details in backup] :

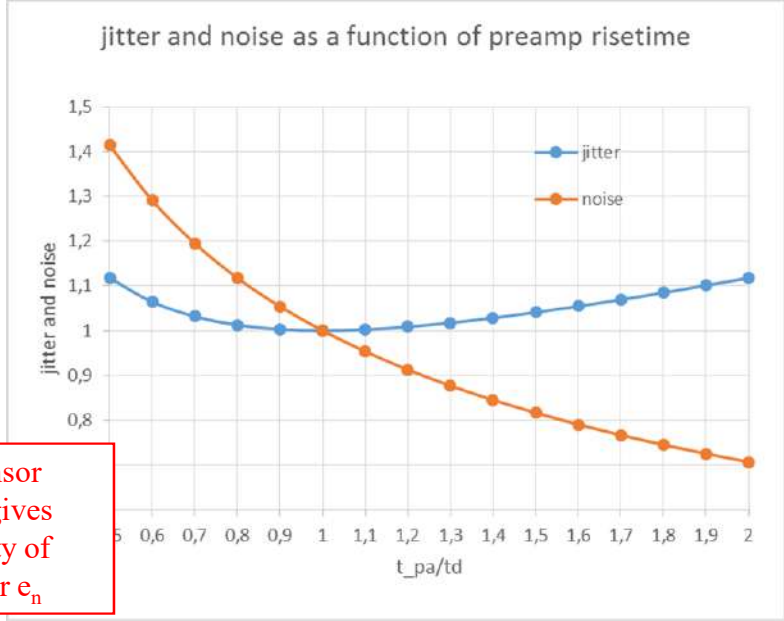
$$\sigma_t^J = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$

- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

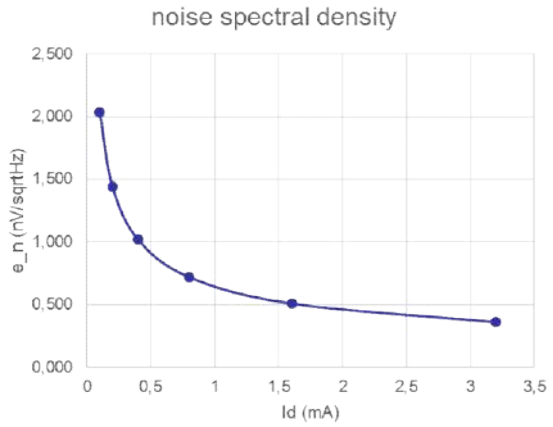
Dominated by sensor Electronics only gives the spectral density of the input transistor e_n



- Gives ps/fC as scales with 1/Qin

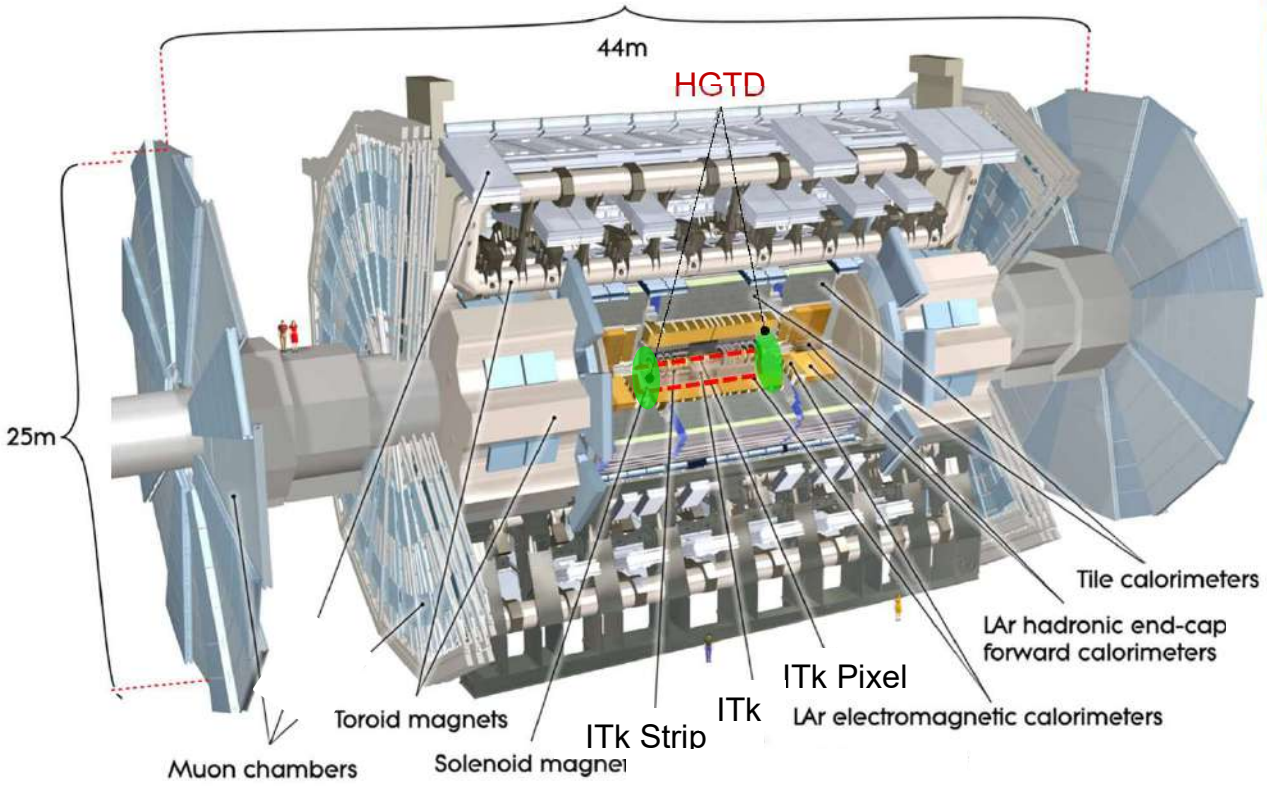
- Electronics noise e_n given by the input transistor transconductance g_m:

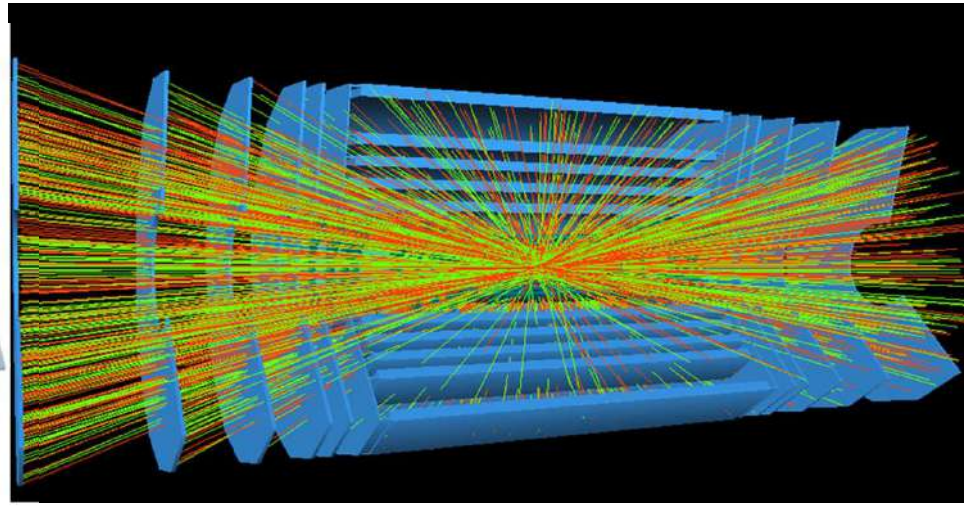
$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$

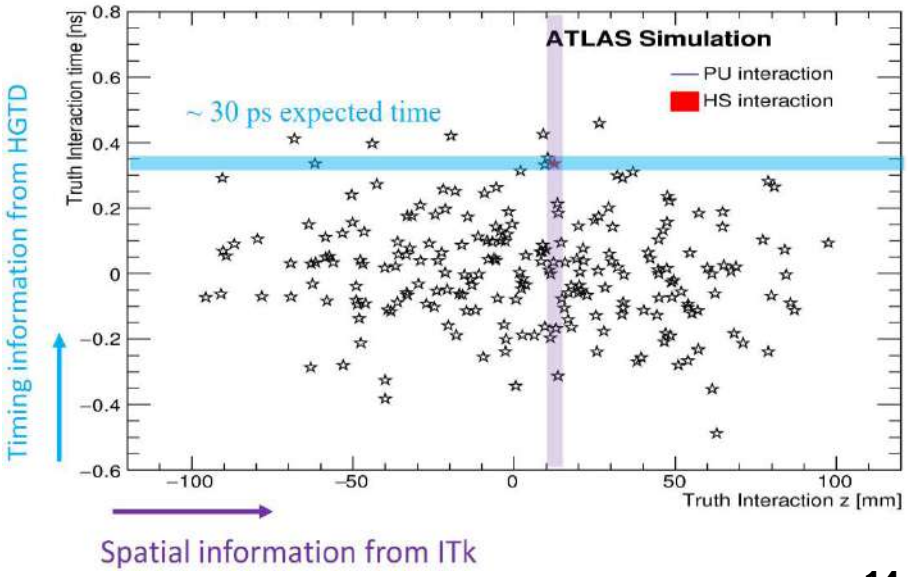


- Expectation : 10 ps for Q=10fC @ C_d=2 pF e_n=2 nV/√Hz t_d=0.5 ns

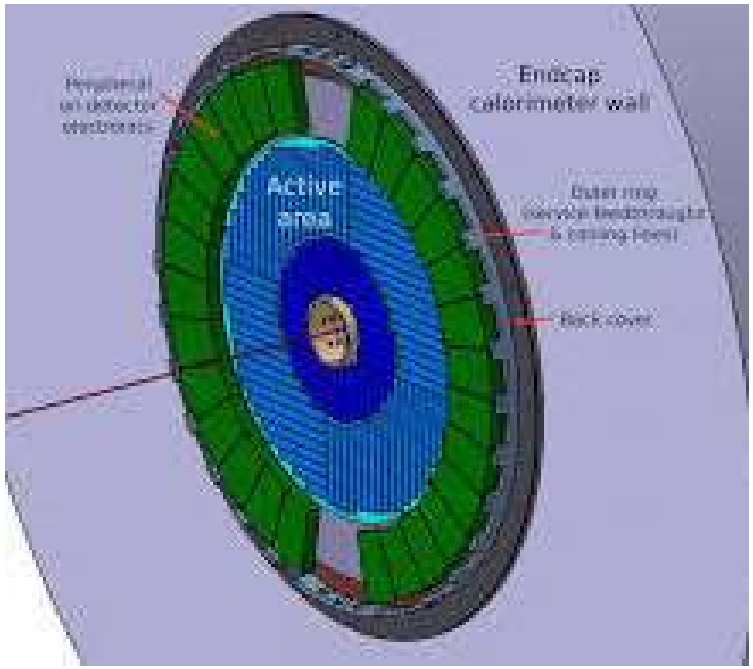
HGTD : new MIP timing detector in ATLAS at CERN



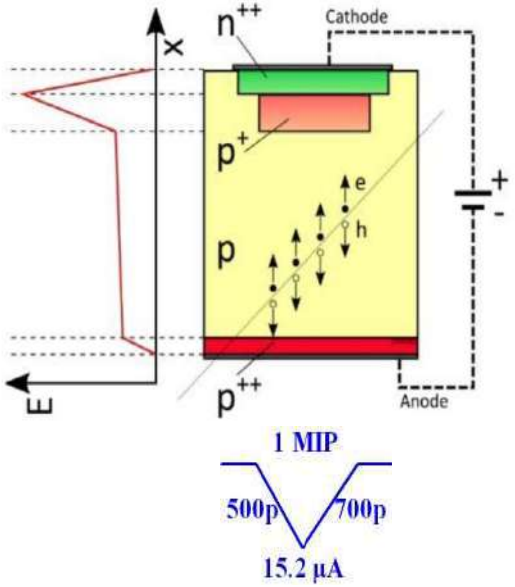


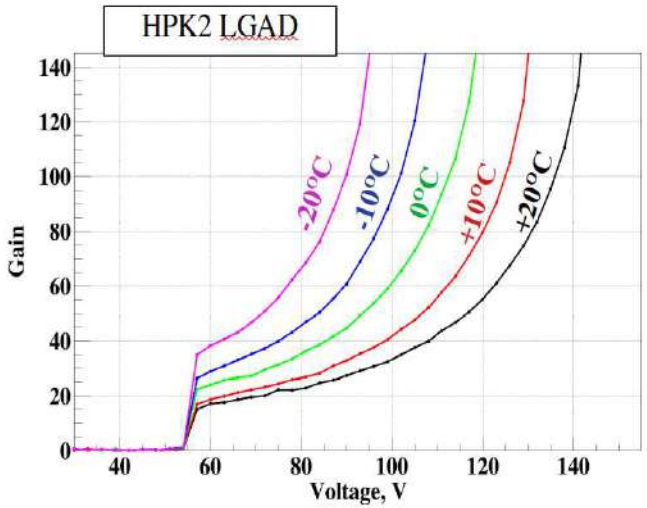


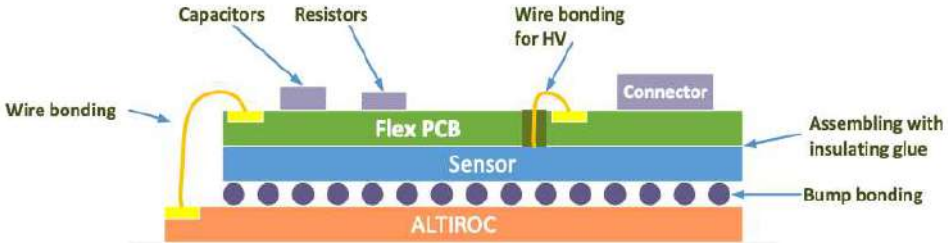
HGTD : Low Gain Avalanche Diodes



LGAD sensors
1.3 x 1.3 mm^2
Thickness = 50 µm

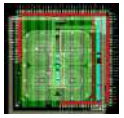






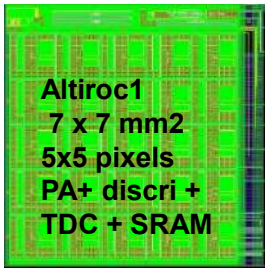
ATLAS LGAD readout : ALTIROC (TSMC 130n)

2016



Altiroc0
2 x 2 mm2
2 x 2 pixels
PA + discri

2017

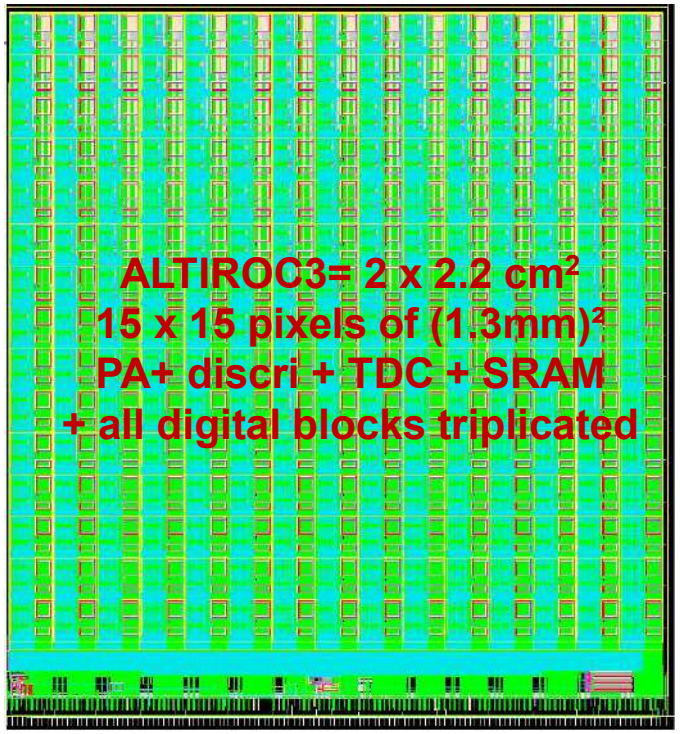


Altiroc0 and 1:
No digital,
To validate the FE part at system level (= ASIC bump-bonded onto a sensor)

2019

ALTIROC2:
First full size chip with 15 x 15 channels – 2 x 2 cm2
To demonstrate the functionality/performance of the ASIC (time resolution + luminosity counting) alone and bump-bonded onto a sensor
But NOT to be fully radiation hard (against SEE)

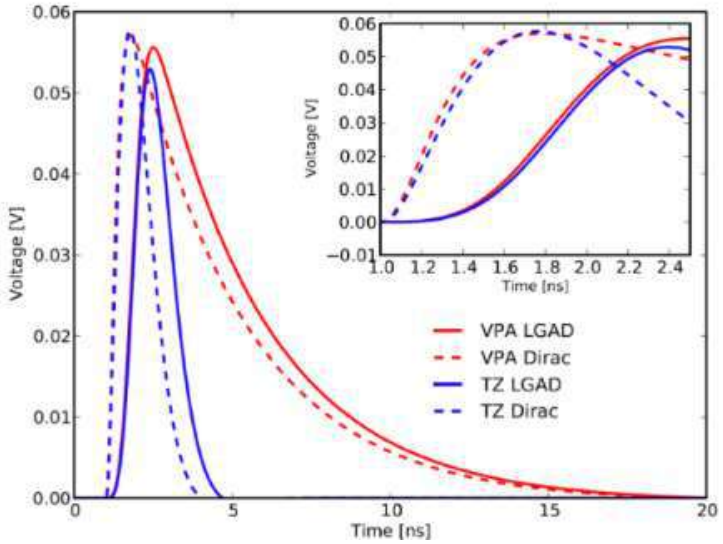
2022

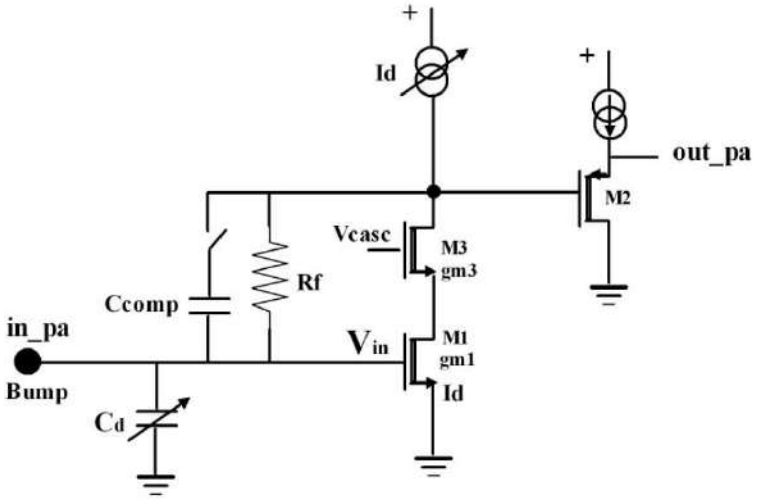


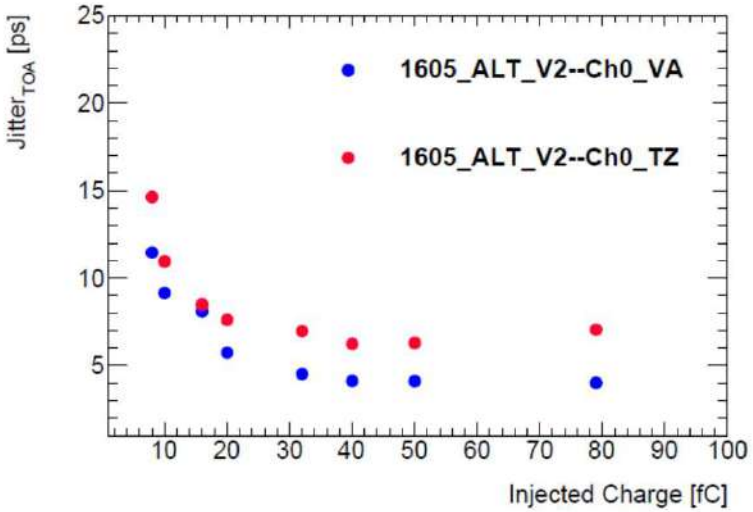
ALTIROC3:
Last full chip prototype before pre-production
Same as Altiroc2 but fully triplicated

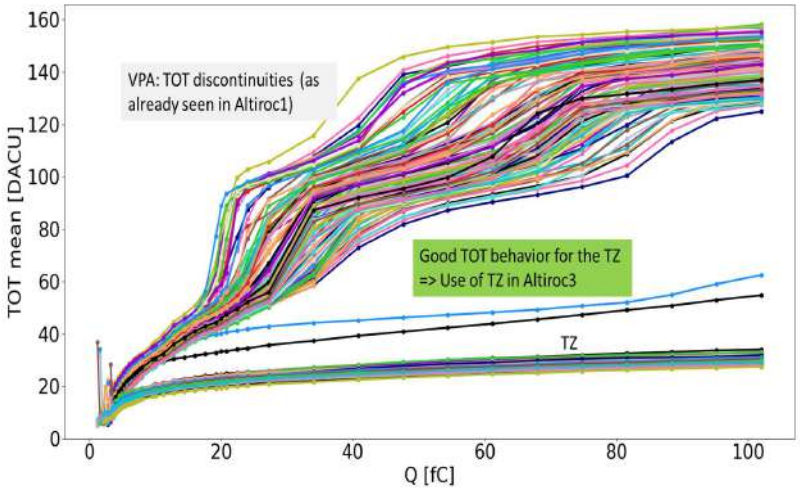
ALTIROC1 : voltage and TZ preamps, test pulse

- « voltage » PA (VPA)
  - Rf = 12k/25k
  - G0 ~ 26 dB
  - Less parallel noise
- Transimpedance PA (TZ)
  - Rf = 4k (+opt Cf)
  - G0 ~ 50 dB
  - Shorter occupancy
  - Better ToT
- Test-pulse
  - « delta » via Ctest : optimistic
  - Rtest added in series
  - Slower rise-time (matche to LGAD pulse)

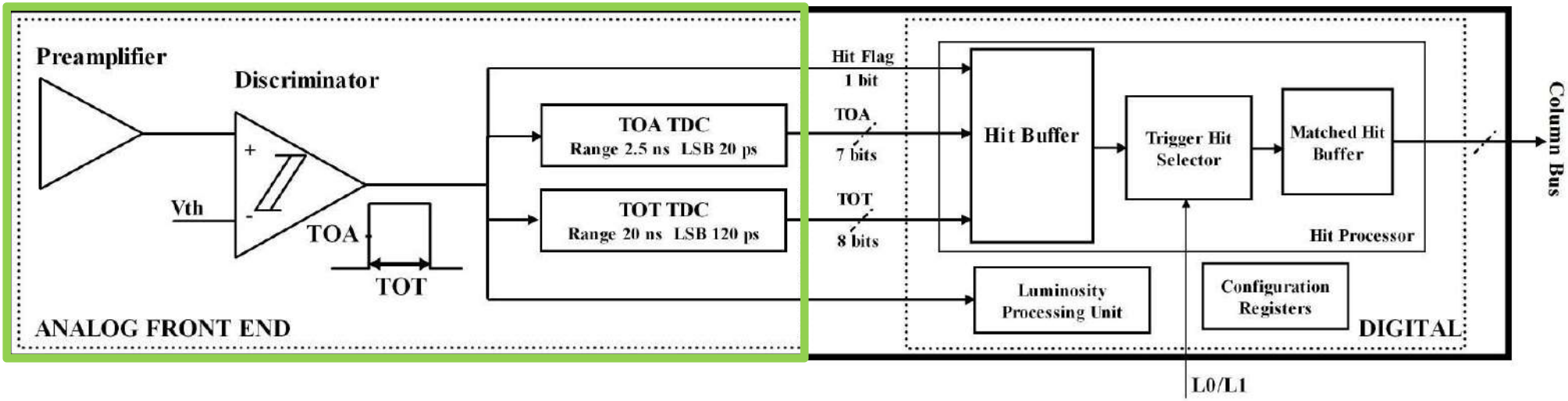








ALTIROC2 : pixel analog front-end



ALTIROC pixel integrates :

- A voltage (VPA) or trans-impedance (TZ) **1 GHz preamplifier** followed by a high-speed **discriminator**:
  - Time walk correction made with a Time over Threshold (TOT) architecture
  - Main challenge = small jitter (low noise/capacitance) down to 4 fC
  - $Q_{MIP}/Cd \sim 1$ mV

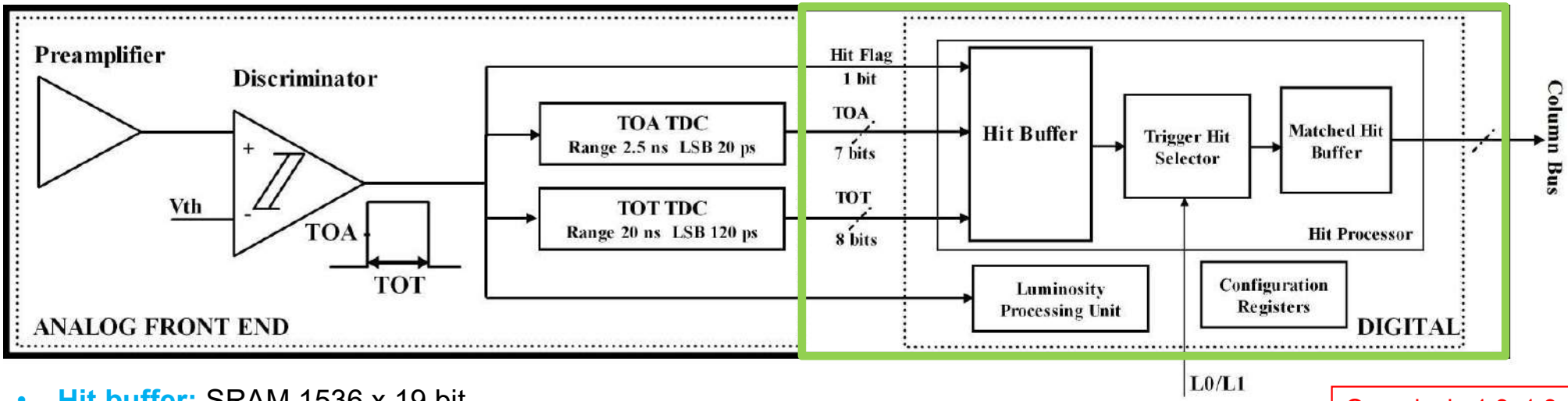
  ⇒ **Analog FE performance crucial**

$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

C_d: sensor cap (~4 pF)
t_d: LGAD drift time, 600 ps
Q_{in}: MIP charge (10 fC at start, 4 fC at end)
e_n: noise spectral density of input trans.

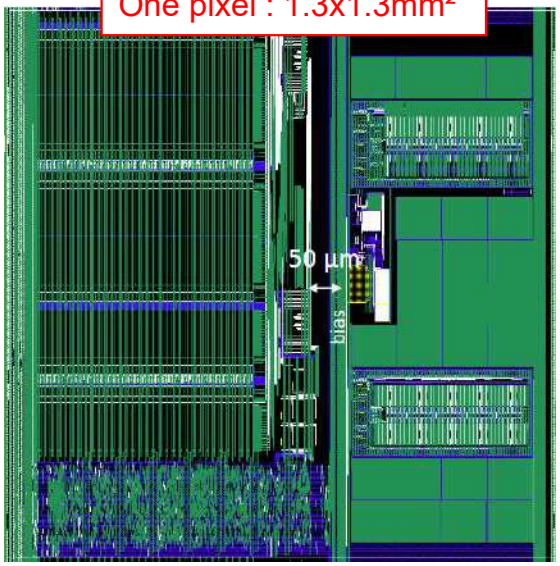
- **Two TDCs** (Time to Digital Converter) to provide Time of Arrival (TOA) + Time Over Threshold (TOT) measurement
  - TOA TDC: bin of 20 ps (7 bits), range of 2.5 ns, to be centered on the bunch crossing
  - TOT TDC: bin of 120 ps (8 bits), range of 20 ns

ALTIROC2 : pixel digital back-end



- **Hit buffer:** SRAM 1536 x 19 bit
  - Circular buffer to store timing data for each bunch-crossing, until a L1 trigger arrives
  - Data = TOT and TOA bits, only in case of hit to save power ; with zero suppress.
  - Depth of about 38 µs
- **Trigger Hit Selector:**
  - Each received trigger associated to a trigger tag
  - If data stored in Hit buffer related to received trigger, TOA/TOT data + trig tag stored into Matched Hit Buffer
- **Matched Hit Buffer:** 32 positions FIFO
  - Control Unit: looks for data related to a trigger event when requested by the End Of Column
  - Matched flag handled through a priority OR chain. Pixel at the top of the column with highest priority
  - Synchronous readout at 40 MHz
- **Luminosity process unit**
  - checks if hits are within 2 programmable windows
- **I2C configuration registers**

One pixel : 1.3x1.3mm²



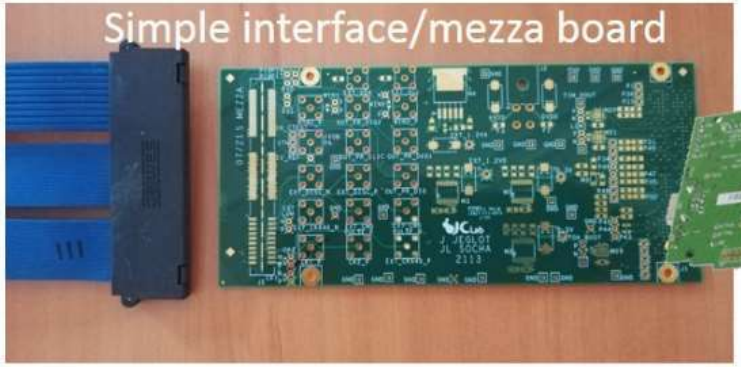
Testbench for ALTIROC2

- Setup = ASIC board (ASIC alone or bump bonded onto sensor) + interface board + FPGA board

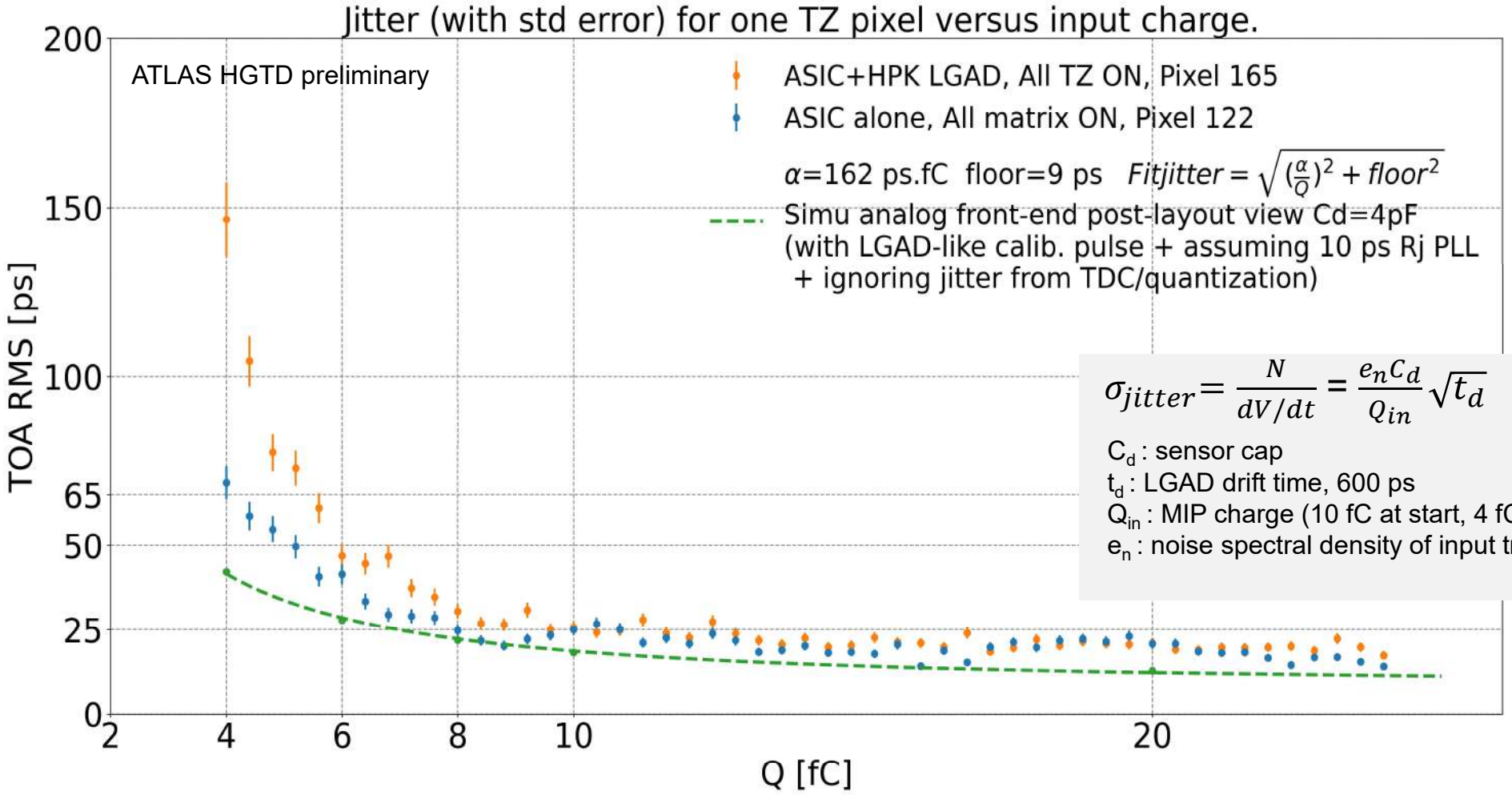
- **Front-end calibration :** charge injection (0 up to 50 fC) using **ASIC** **internal calibration pulser**, controlled by the FPGA, synchronous to 40 MHz clock, ASIC alone: Cd=3,5 pF can be set by SC to mimic sensor capacitor

- **TOA/TOT TDC calibration :** ASIC periphery generates a trigger with tunable width and delay thanks to the phase shifted 640 MHz clock from the PLL + Random Phase Generator for DNL

Interface + FPGA board



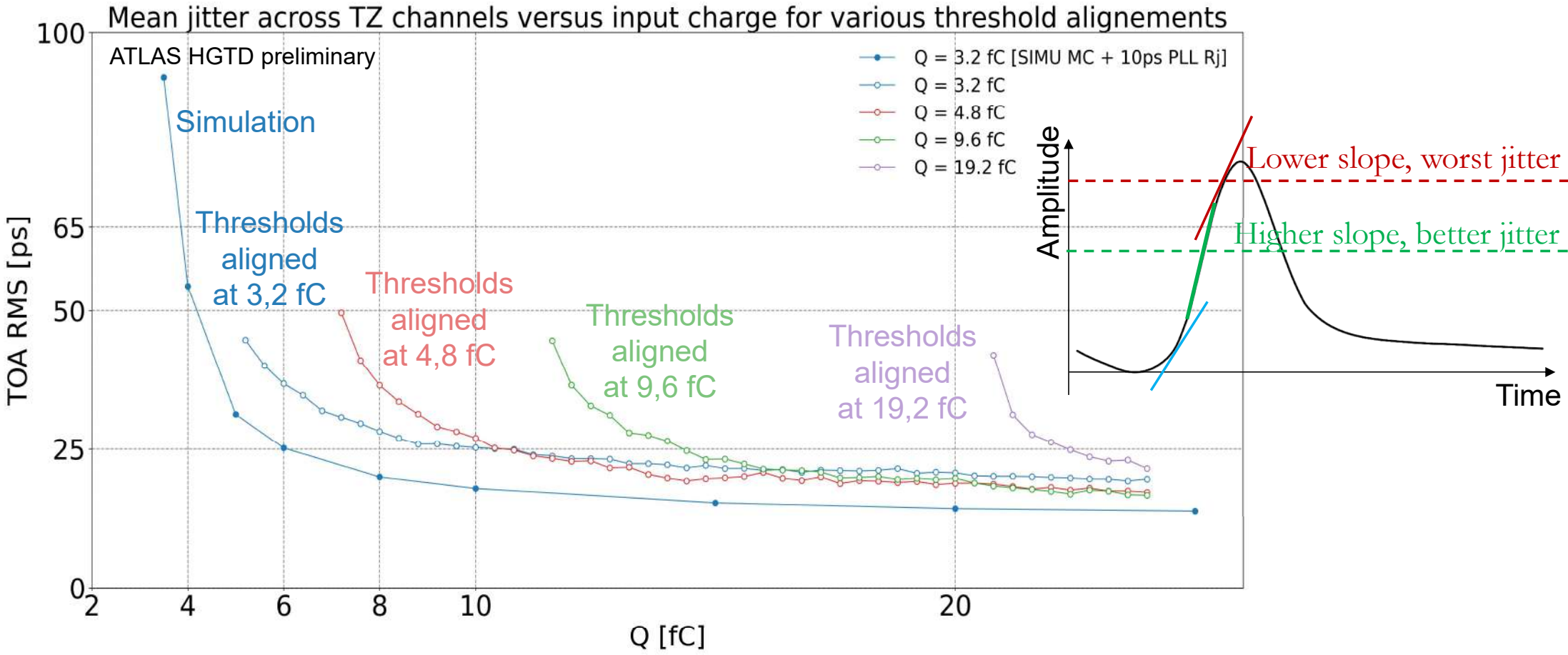
Comparing measured time-of-arrival jitter with simulation



$$\sigma_{jitter} = \frac{N}{dV/dt} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

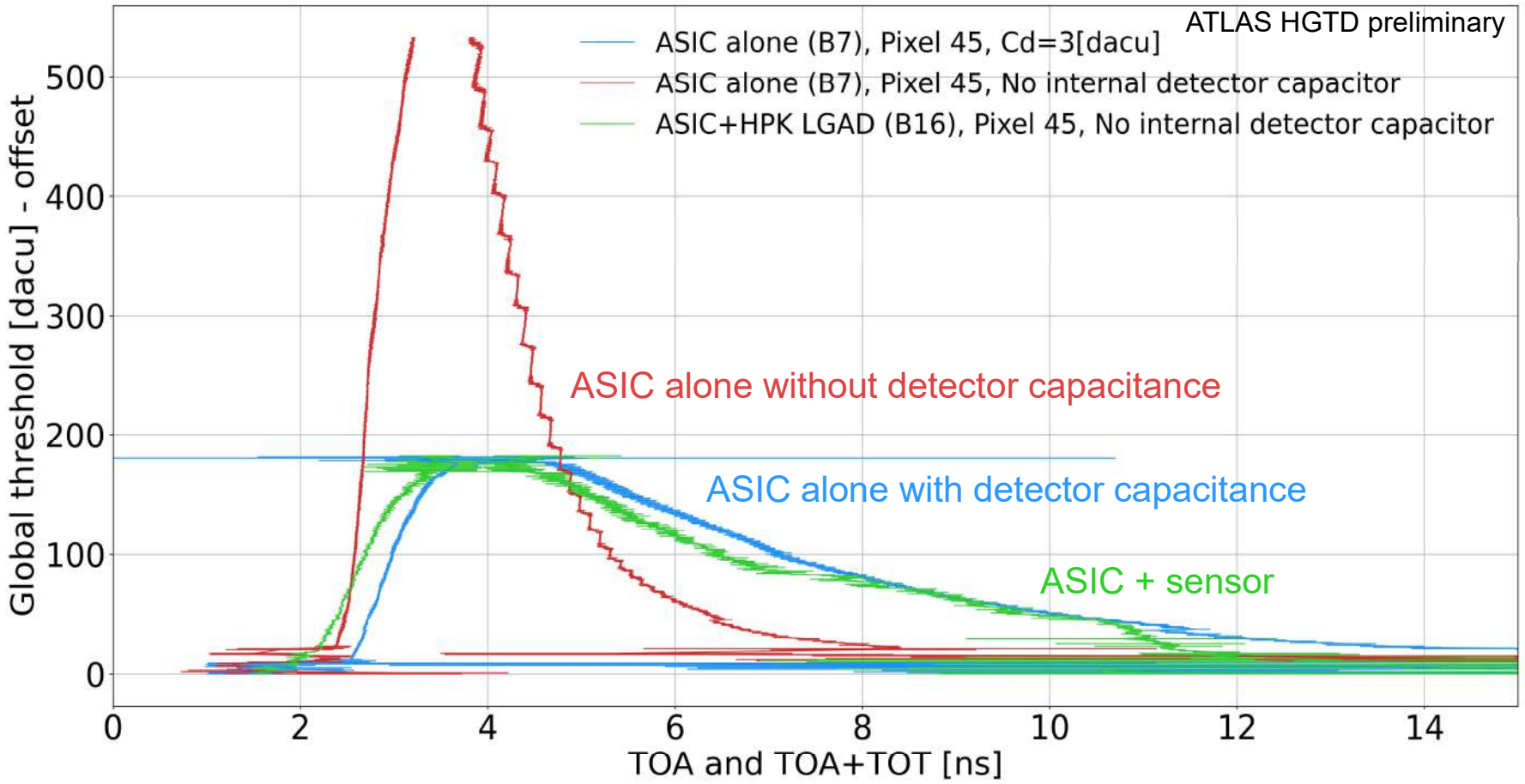
C_d : sensor cap
t_d : LGAD drift time, 600 ps
Q_{in} : MIP charge (10 fC at start, 4 fC at end)
e_n : noise spectral density of input trans.

Jitter depends on the charge, but also on the discriminator thres.



Threshold trade-off to maximise pulse slope (dV/dt), thus minimize jitter.

Is the internal detector capacitance equivalent to an LGAD's ?

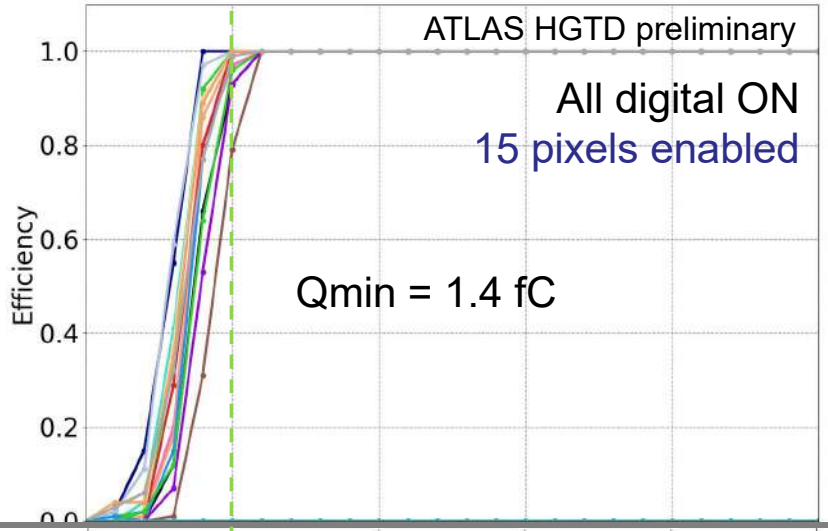


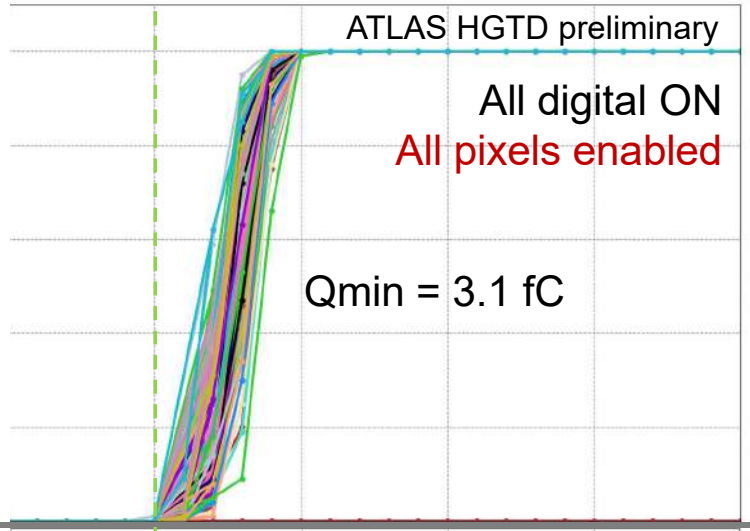
with calibration pulse

Pulse reconstruction of a voltage preamplifier, between ASIC alone and ASIC + sensor :
Showing same amplitude & falling edge decay time → the internal LGAD-like capacitance corresponds to 3.5 pF.
Showing slightly slowly rising time → partially explains worst jitter with sensor.

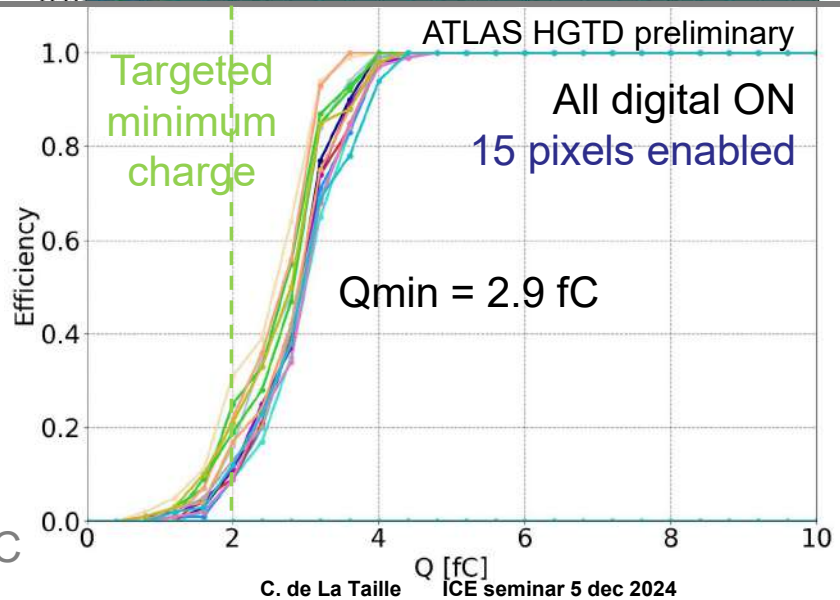
What is the minimum detectable charge ? (Median at 50%)

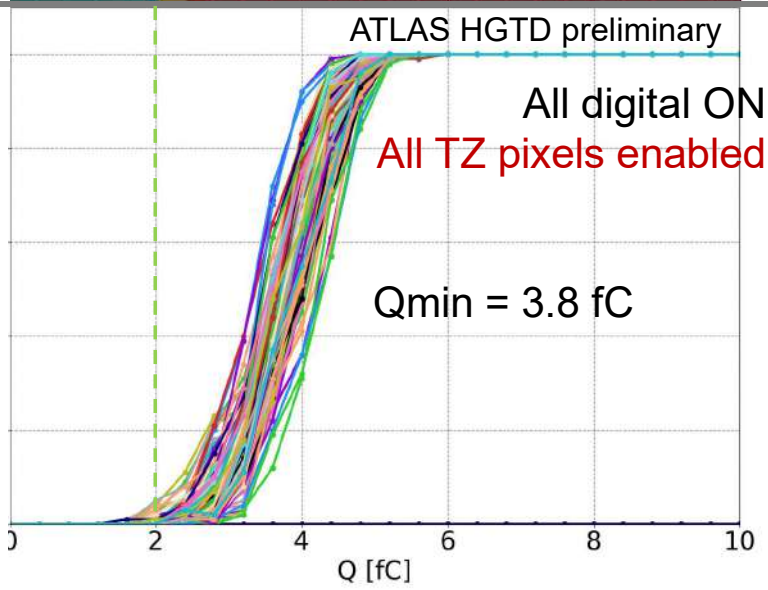
ASIC alone
irradiated up to 200 Mrad





ASIC + LGAD
(unirradiated)





Transimpedance preamplifier results
Thresholds aligned at 3.2 fC

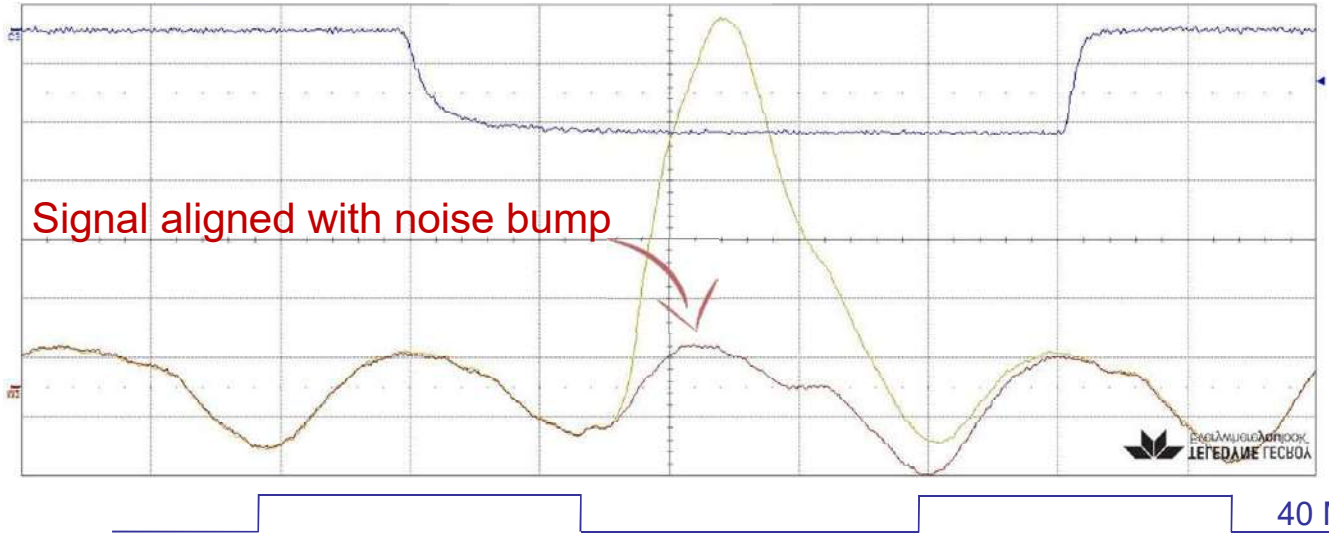
Fighting against digital activity

Probing one transimpedance preamplifier :

20 fC injected
Signal = 30 mV

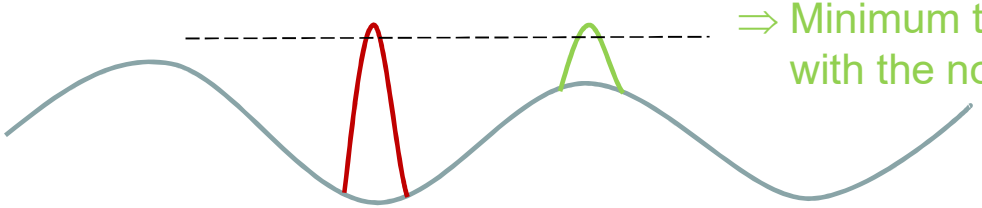
ASIC+HPK LGAD biased at -80V (B16)

profit that the signal is synchronous with the clock



Digital clock couples on preamplifier gnd input : induces a noise ripple ~ 3 fC = our limit !

Preamplifier output baseline : (exaggerated)

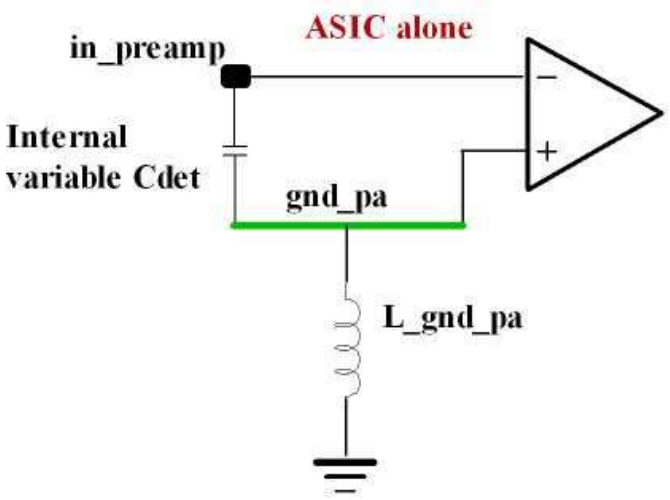


⇒ Minimum threshold obtained aligning the signal with the noise bump.

⇒ Signal amplitude seen by the discriminator reduces : “hidden” inside the noise ripple !

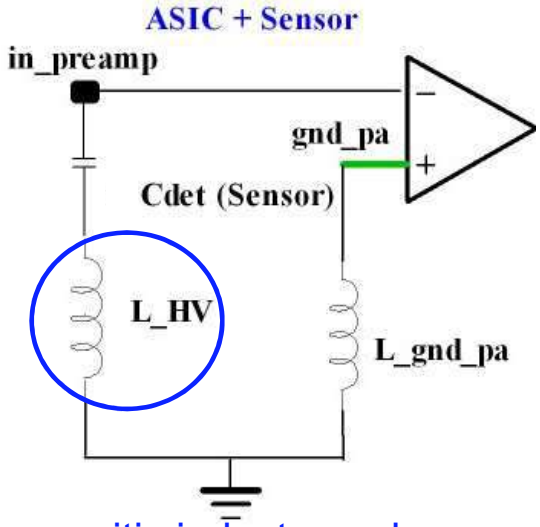
Sensor effect on noise

One channel



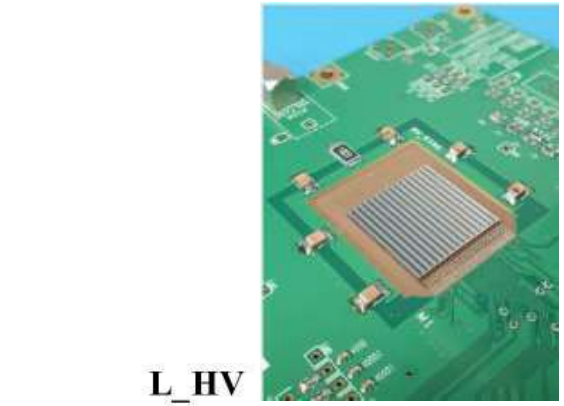
Noise on analog gnd amplified x1
"common mode"

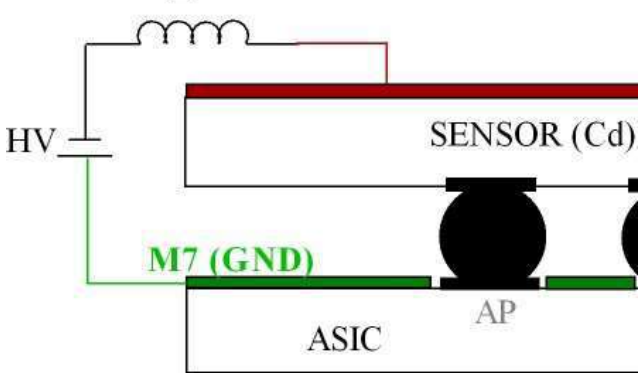
ASIC alone = favourable situation



Can this parasitic inductance be hidden from the preamplifier ?

Noise on gnd_pa amplified x20
"differential mode"

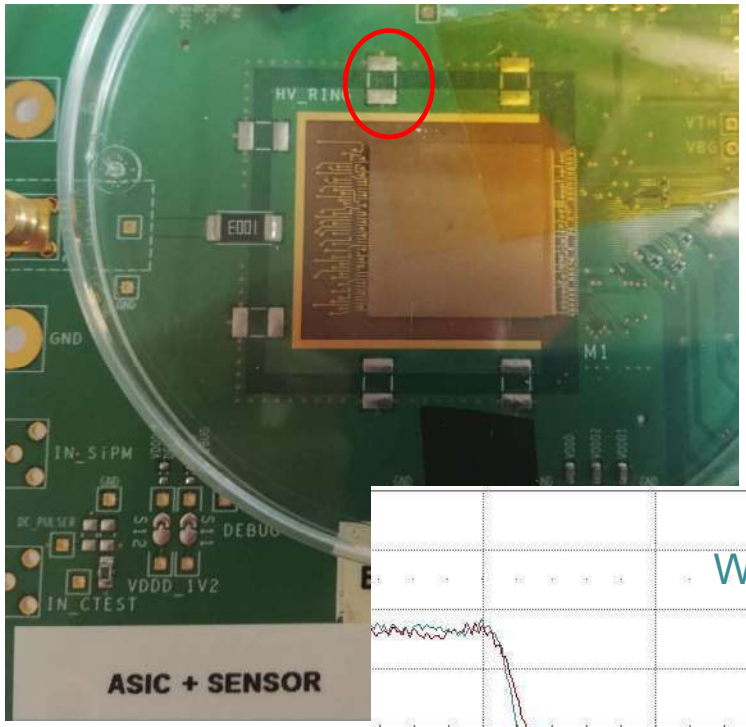


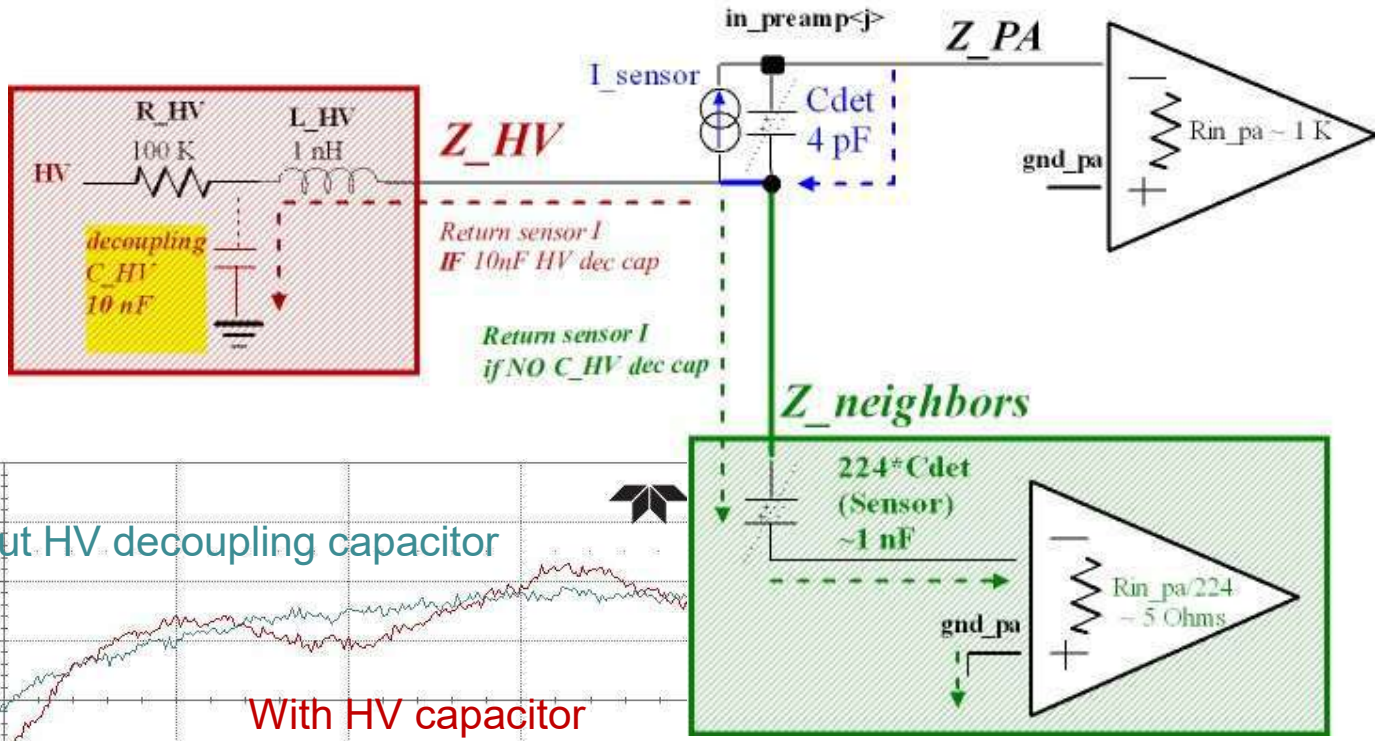


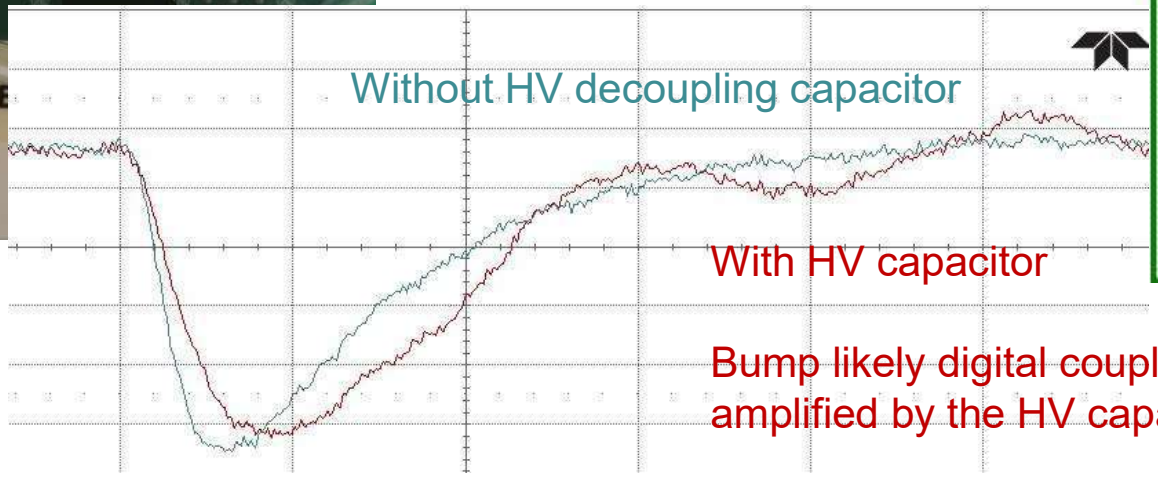
Digital noise injected on the preamplifier ground gets amplified only when the impedance between the detector capacitance and the non-inverting preamplifier input is not zero : when the sensor is connected !

Effect of HV decoupling : where is the AC current flowing back to ground ?

10 nF HV decoupling capacitor adds 50% more noise on a TZ output.







Bump likely digital coupling inside the asic amplified by the HV capacitor

Optimal HV impedance is very different for 5x5 and 15x15 sensor

- **HV resistance :**
  - varied from 0 to 1kOhm
  - Effect on gnd_pa noise amplification
    - Goes from 20 to 1
    - ~1 for R>100 Ohm
  - Current return ensured by the 224 spectator channels
    - Was not the case with smaller sensor

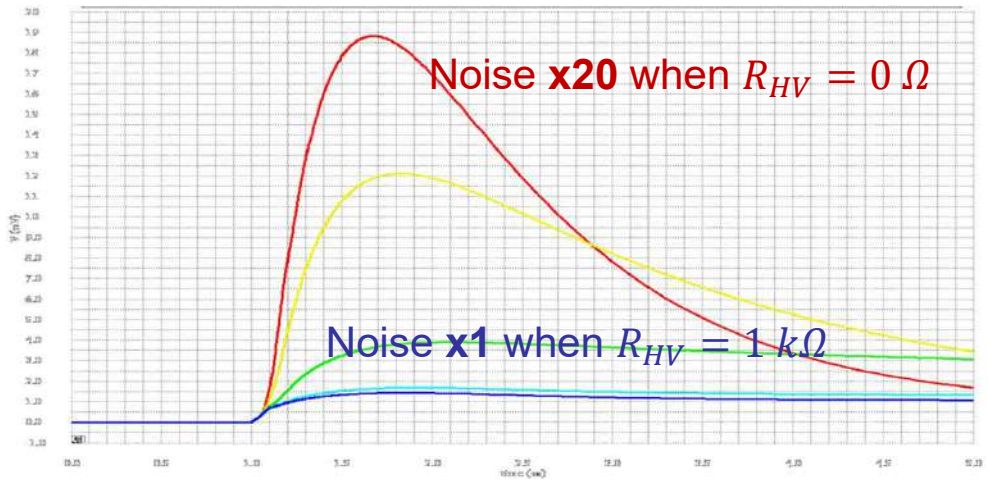
- **HV parasitic inductance :**
  - Effect of 10 nH in HV

  1 channel, 25 channels, 225 channels

  = Altiroc0/Altiroc1/Altiroc2

Altiroc2 doesn't suffer from HV parasitic inductance !

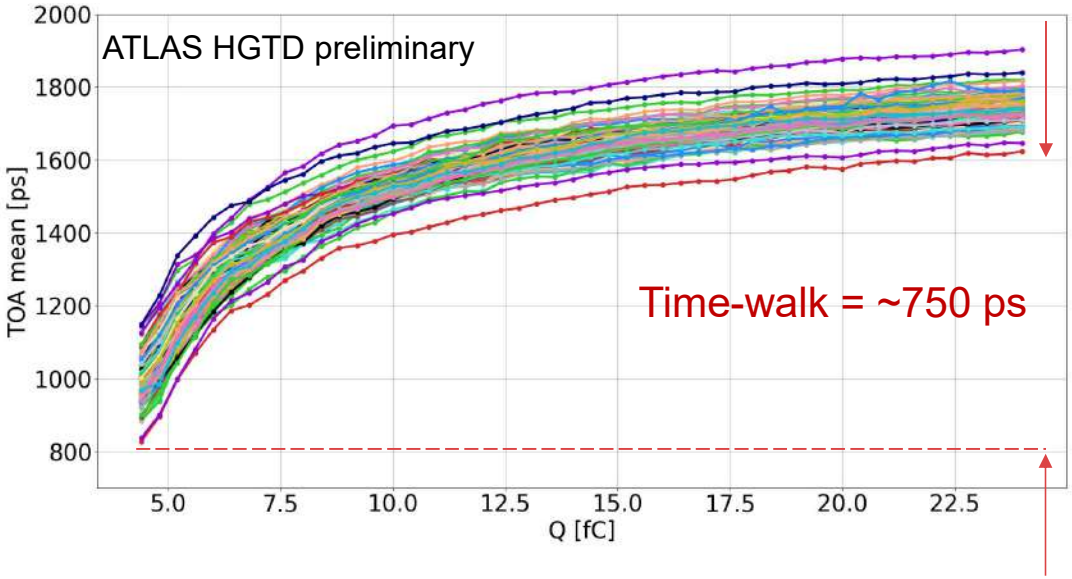
Ground noise amplified by PA as signal



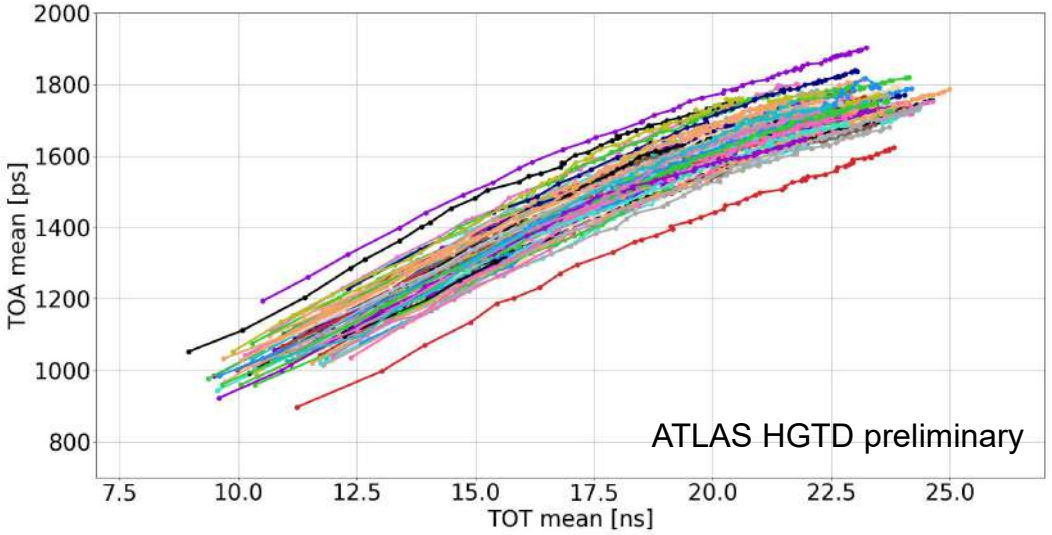
Correcting time-of-arrival timewalk with time-over-threshold

ASIC+HPK LGAD biased at -80V (B16) All TZ ON

TOA versus charge



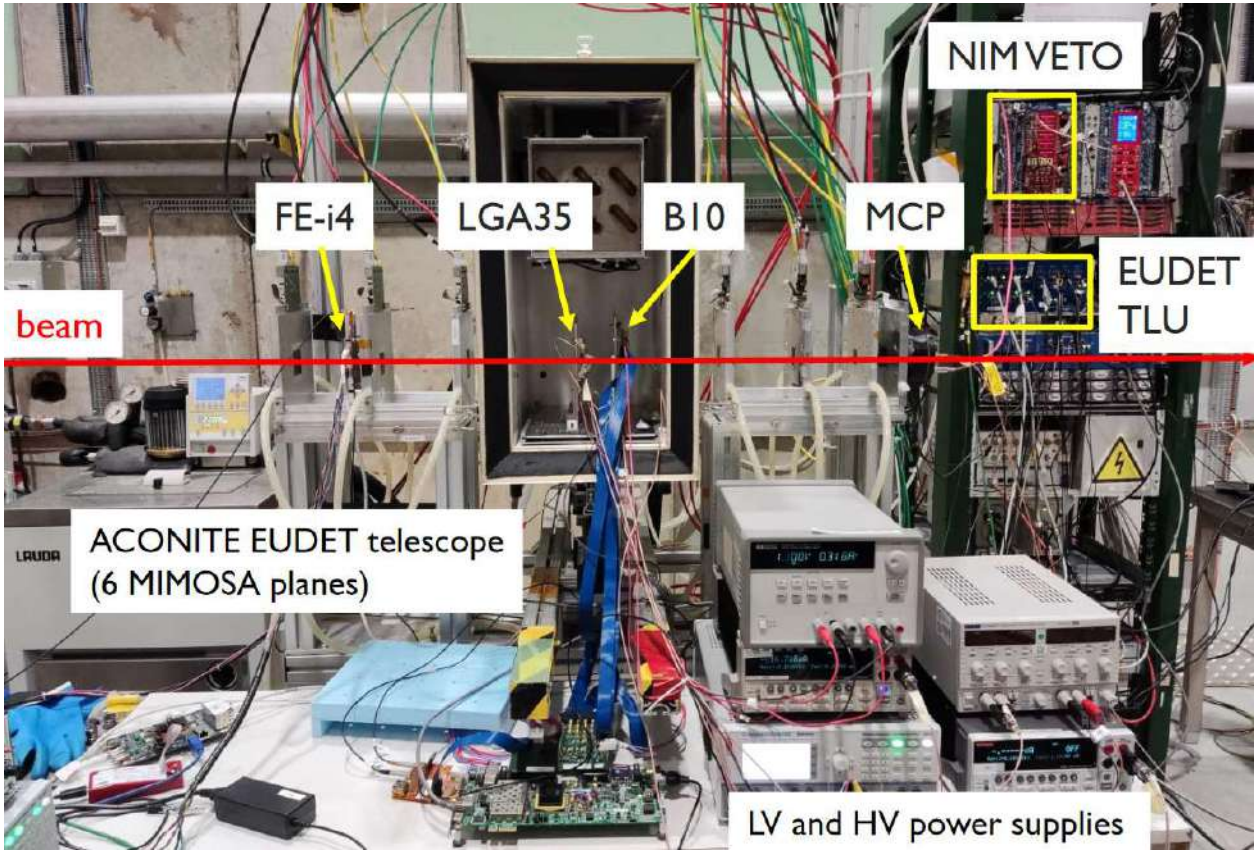
TOA versus TOT



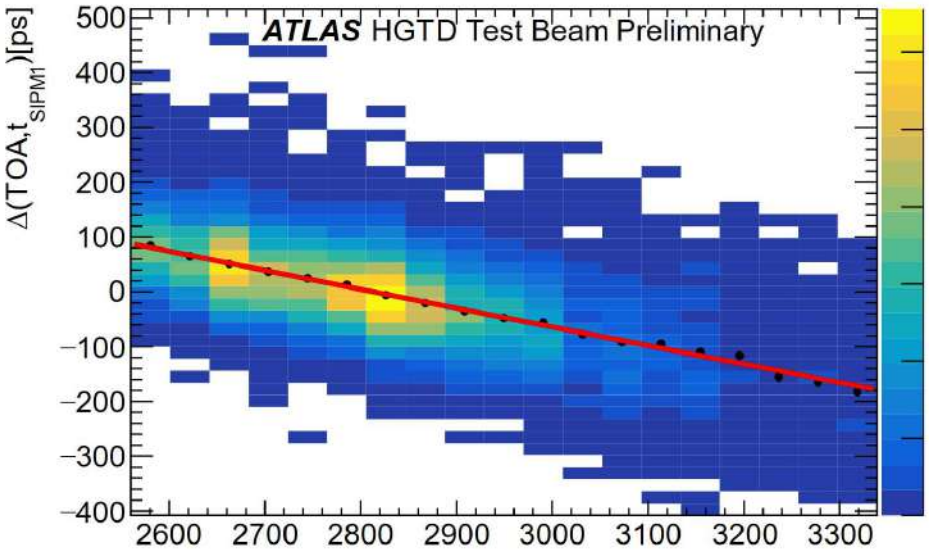
- Time-walk = convolution of the preamplifier rise time (300 ps) with LGAD rise time (600 ps)
- Skew between bottom and top of the column pixel : due to clock tree distribution

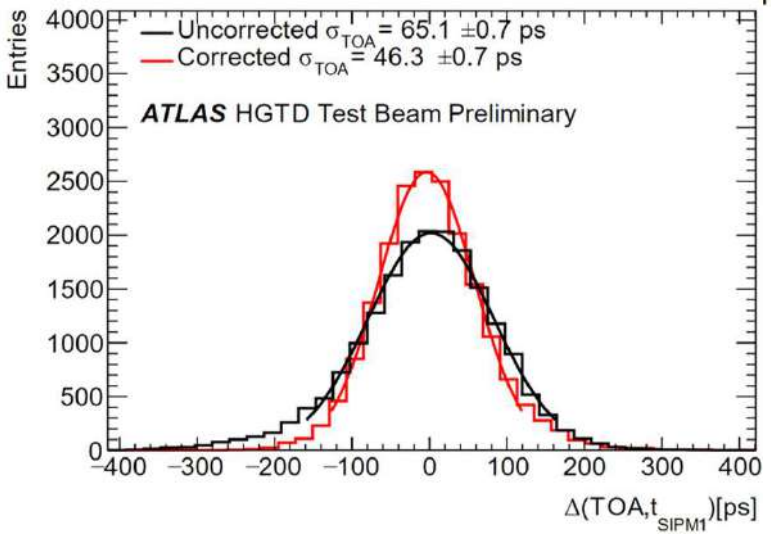
- Offline time-walk correction using TOT

Testbeam measurements (pions)



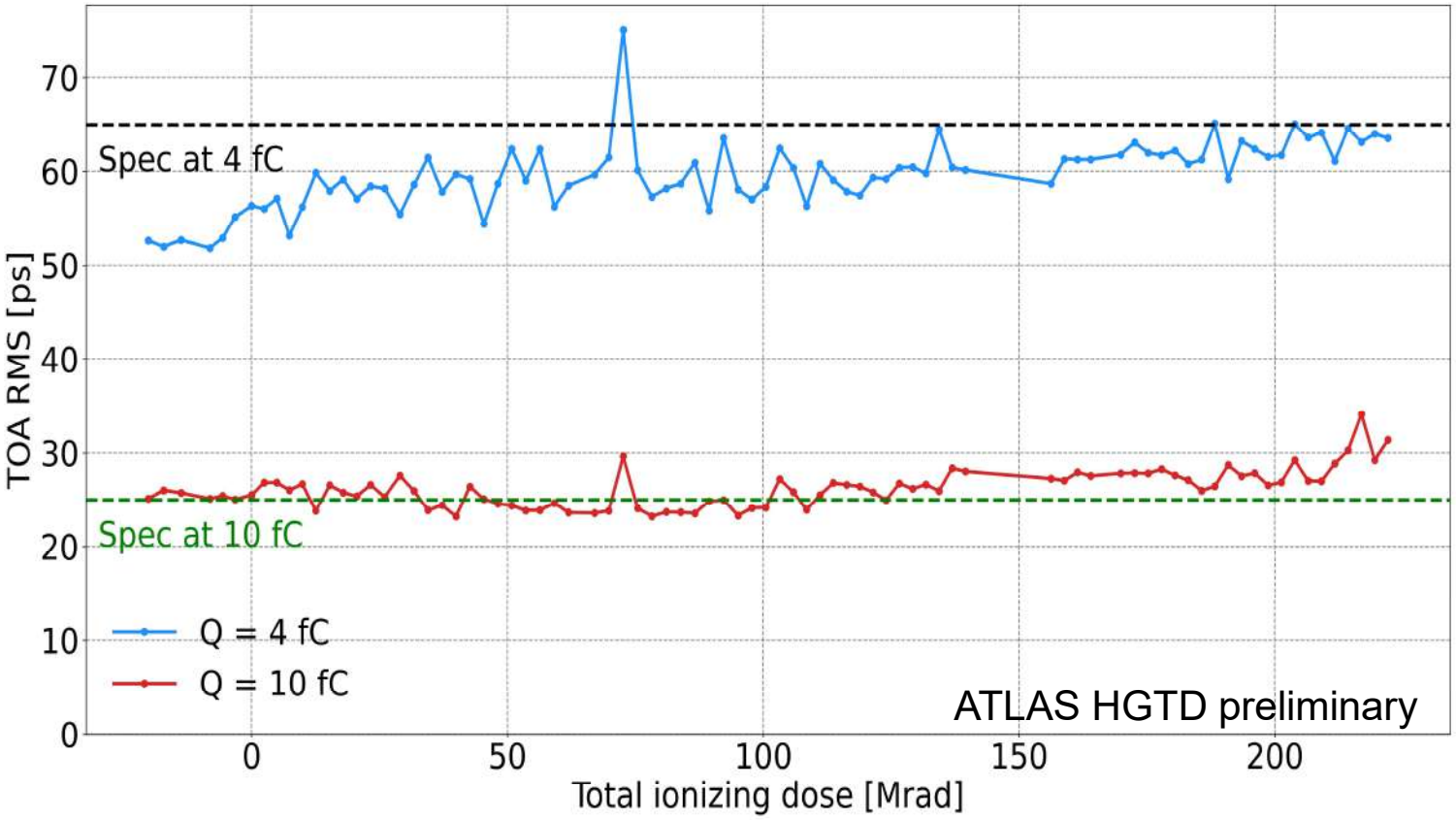
HGTD tests at CERN SPS with ALTIROC2





Jitter stability under TID irradiation

ASIC alone (B7) Pixels ON : Col 7 (VPA) or 8 (TZ)



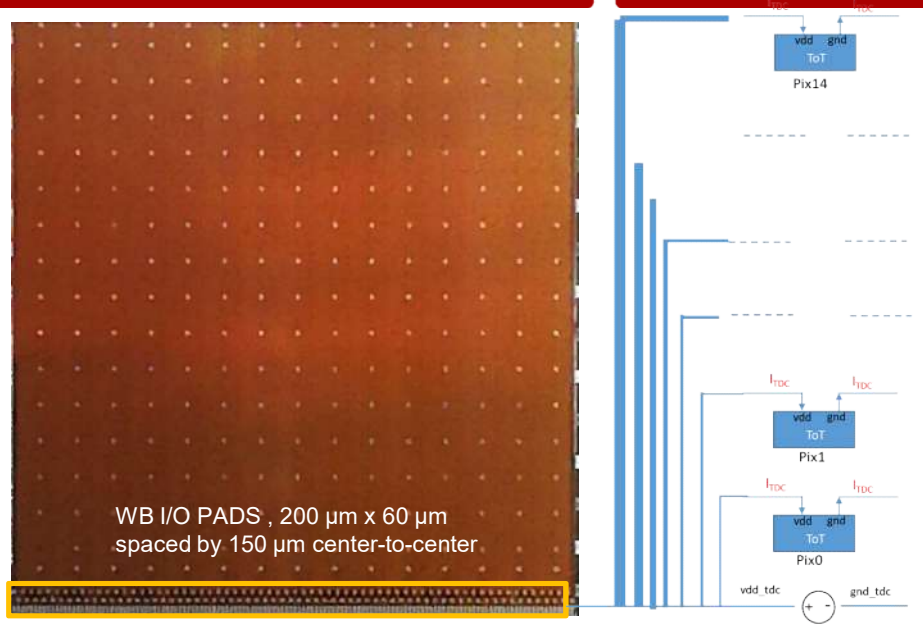
TID : 220 Mrad
Dose rate : 3 Mrad/h
Temperature : 22°C

All DC values and TDC bin remain constant along irradiation.

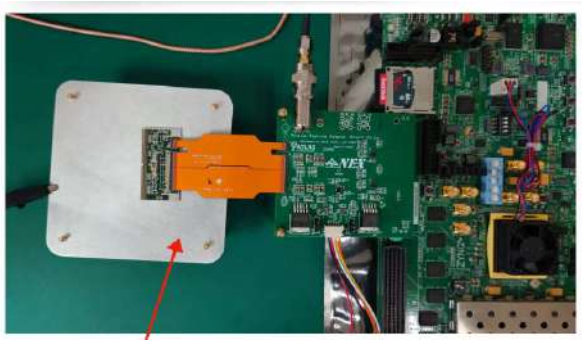
Main challenges: technical difficulties

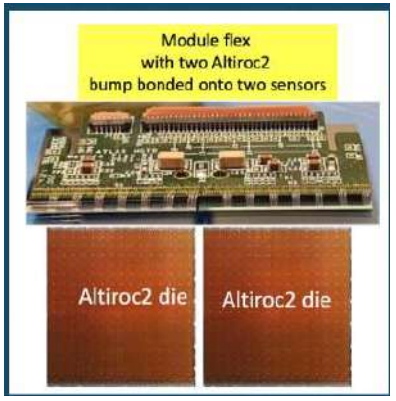
- Large chip (2 x 2 cm2) powered on one side only => sensitivity to IR drops

- Very delicate floorplan to be done to guarantee the analog performance
  - Ultra Low impedance for the ground of the preamp crucial
  - **Several power domains**:
    - Specific power lines for each analog/mixed block: vdd_pa/gnd_pa, vdd_disc/gnd_disc, vdd_toa/gnd_toa, vdd_tot/gnd_tot
    - For Altiroc3: Vdd_toa, vdd_tot, gnd_toa, gnd_tot per column and then distribution of powers/grounds to each pixel with same R to avoid LSB dependency with activity
    - Specific power lines for digital blocks: vddd/gndd, vddd1/gndd1, vddd2/gndd2



Altiroc3 power/gnd TDC distribution per column





Main challenges: organizational difficulties

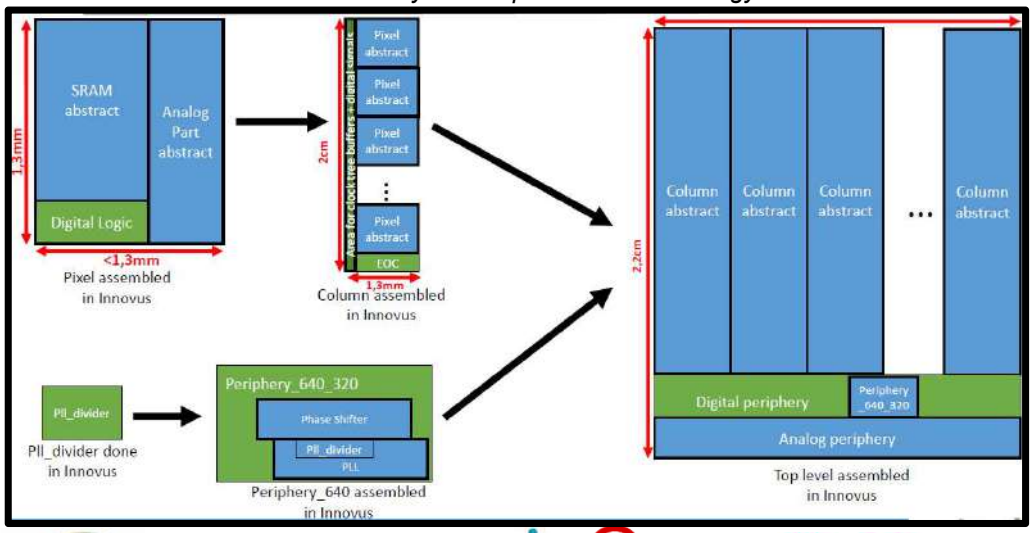
- Organization: Design done by engineers spread in 6 labs – ~ 7.5 FTE
  - SOS, Trello and Mattermost: to ensure quick/"easy" communication but some drawbacks too

- **Analog 30 %** of the chip
  - Analog performance and **Floorplan crucial** to guarantee analog performance at system level
  - 2.5 FTE: Omega (1.8 FTE) , Clermont (0.7 FTE) , SLAC (< 0.1 FTE for TDC) , SMU (< 0.1 FTE for Phase shifter)

- **Digital 70 %** of the chip
  - **Clock Domain Crossing, timings, SEE robustness**
  - 5 FTE: Clermont (2.2 FTE) , Chips (2 FTE) , IFAE (0.8 FTE)

- Assembly done **Full Digital on Top** + UVM verification
  - Top level assembled with INNOVUS
  - Verilog models and lib files to be done for all analog/mixed blocks
  - Analog periphery treated as a macro block

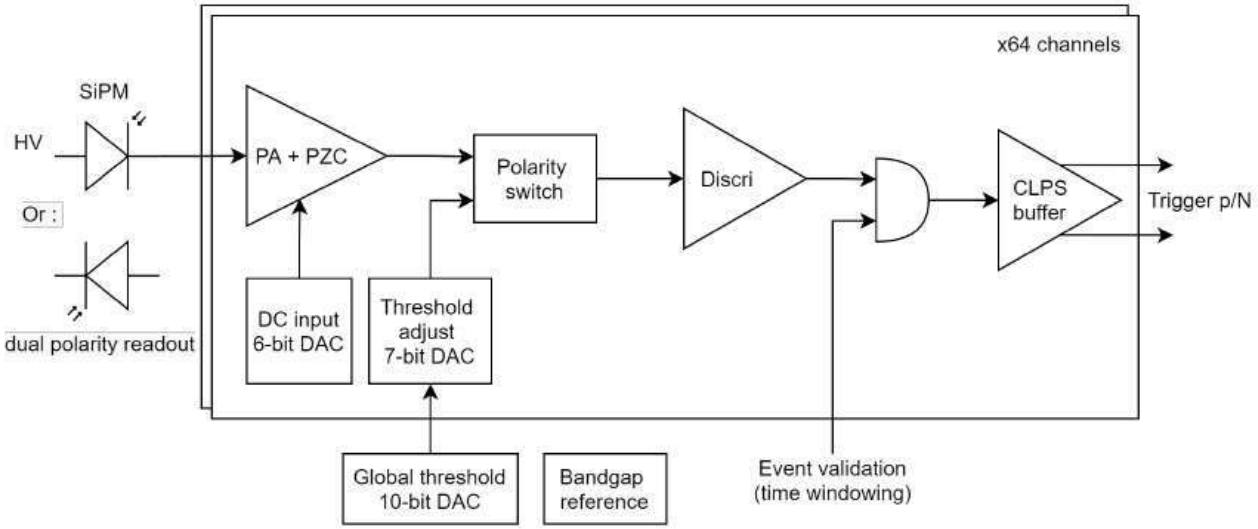
Altiroc3: Physical Implementation strategy

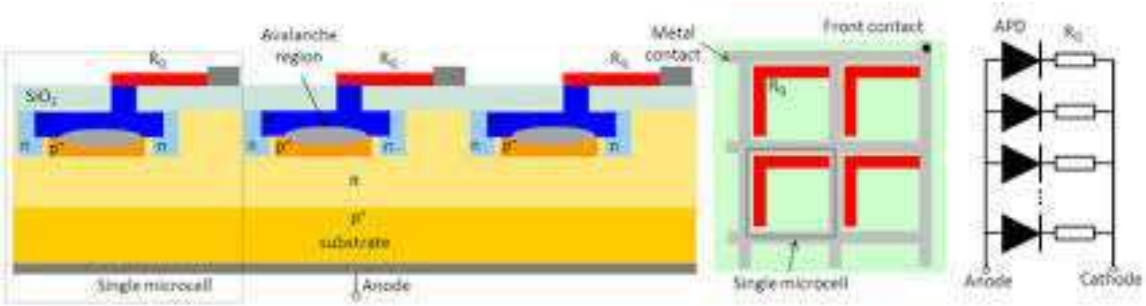


⇒ **Difficulties:**

- Design driven by digital while analog floor plan crucial for the performance
- UVM manpower: mainly at CERN, difficult to recruit UVM engineers at IN2P3
- Any modification, even very minor ones, in the analog or digital part implies that the implementation (layout) of the full chip must be redone + verifications to be redone from the beginning (regressions)

Introducing LIROC : SiPM read-out for Lidar

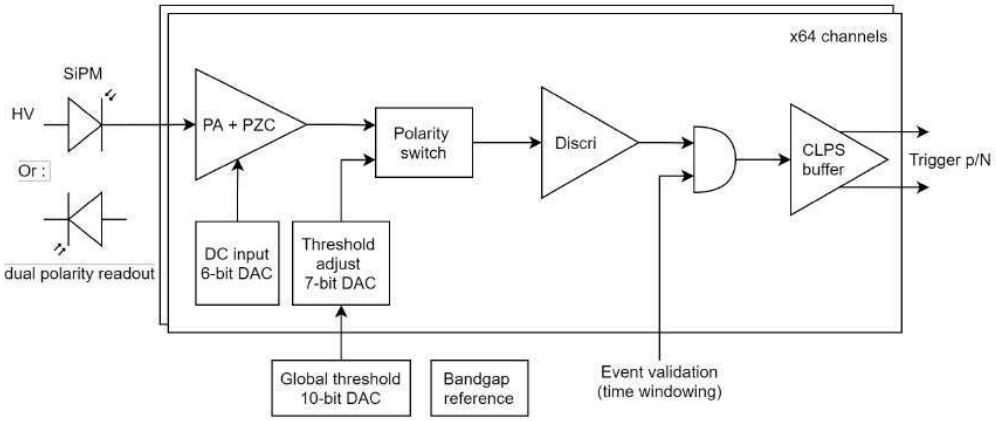


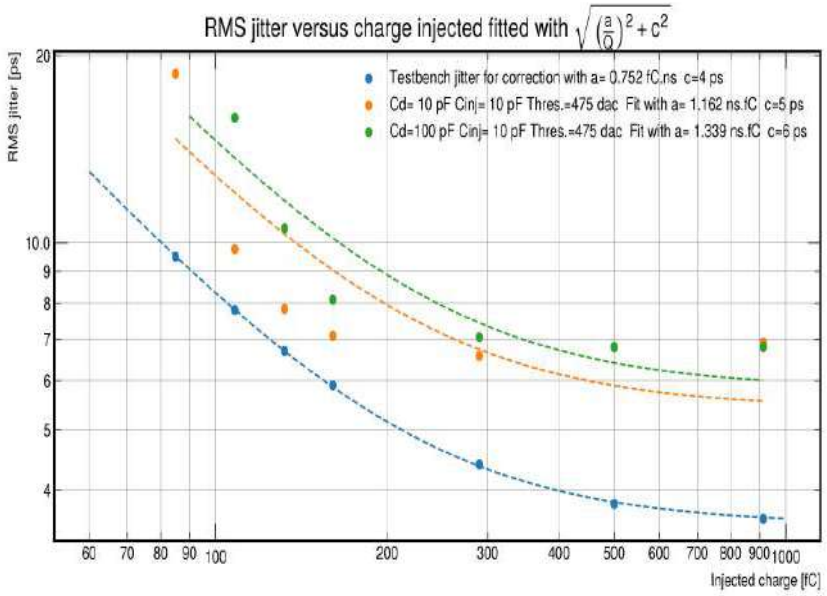


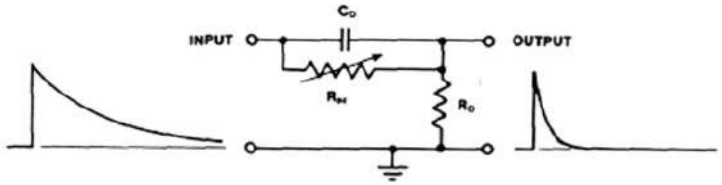
Collaborative design between Weeroc & Omega laboratory that have received Funding from ATTRACT EU H2020 Research & Innovation Program

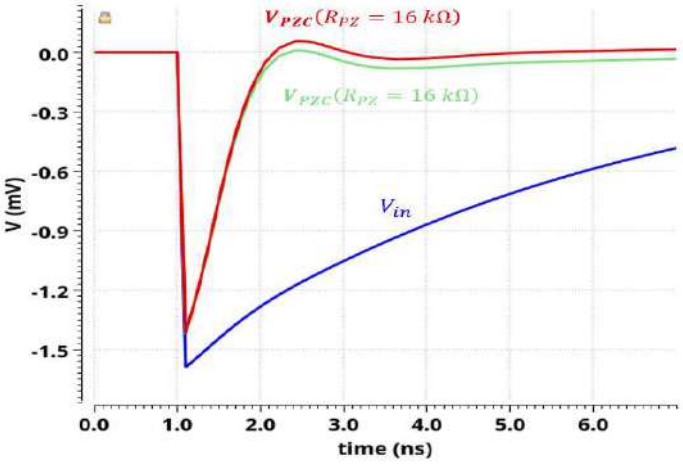
LIROC performance

- LIDAR readout : short double pulse separation
  - 64 channels high speed PA + discri
  - Trigger on 1/3 photoelectron
  - Pole-zero cancellation for 3 ns double pulse separation
  - CLPS discriminator output : couples to picoTDC
  - 3 mW/ch CMOS 130nm

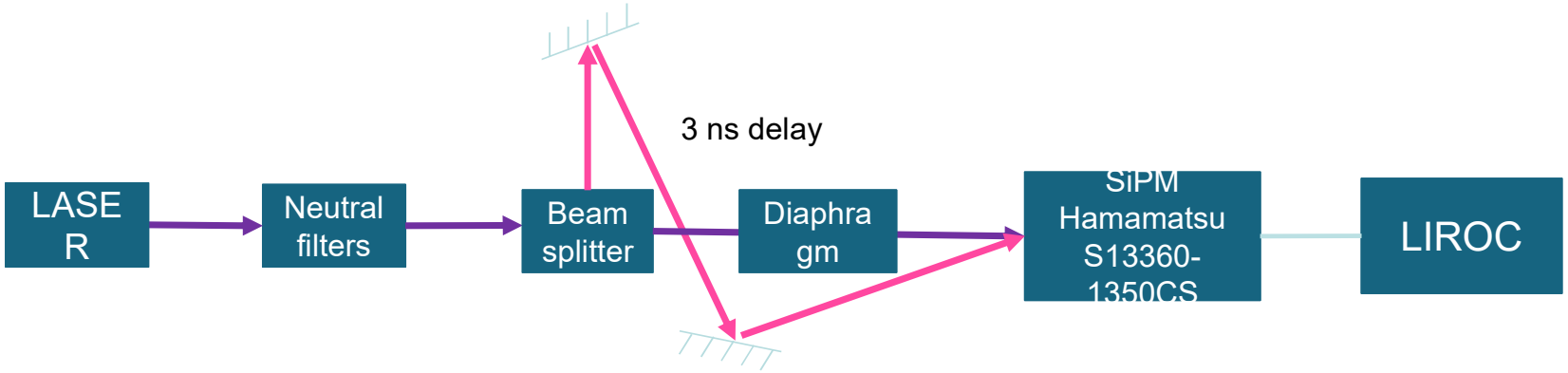


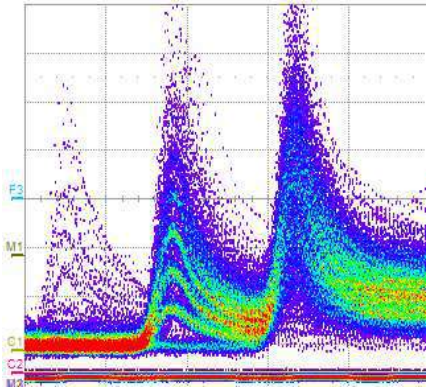




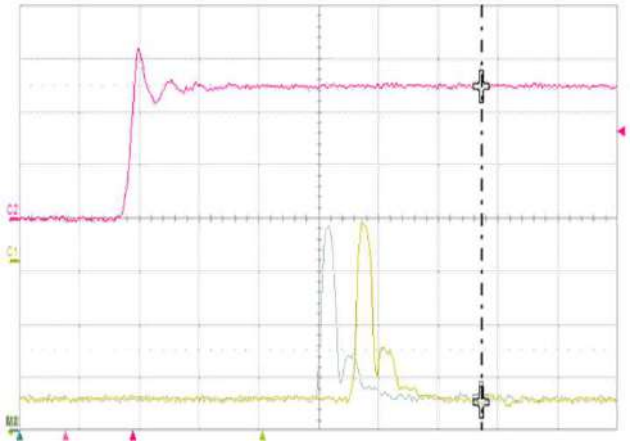


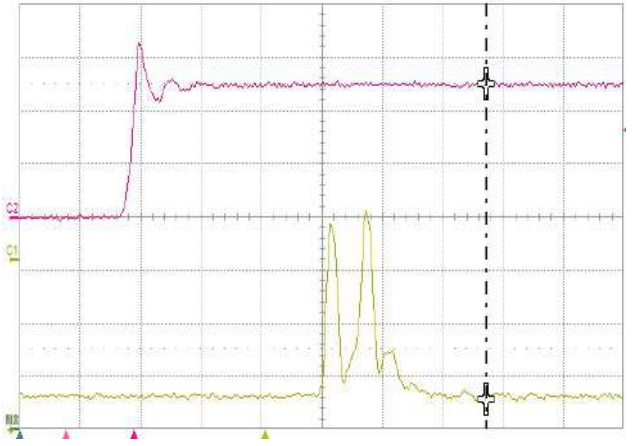
LIROC : double pulse separation



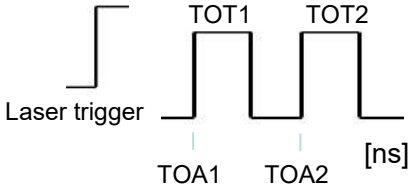


Direct to oscilloscope, 3 ns interval



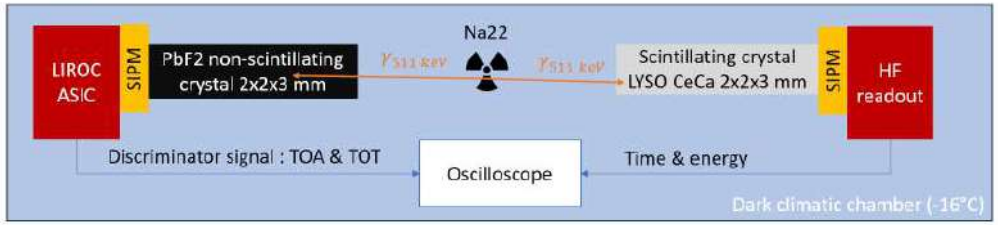


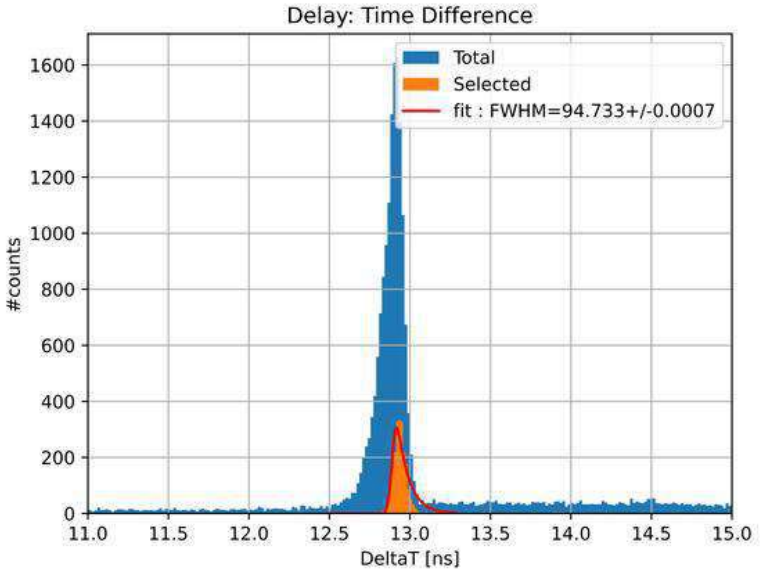
50 mV/div
5 ns /div

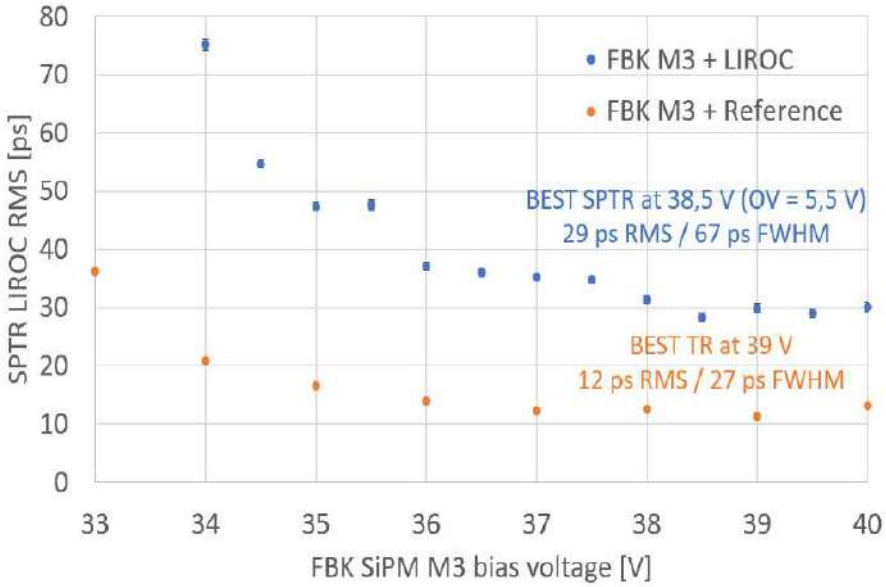


Conclusion : 3 ns double pulse well separated

LIROC Single Photon Time Resolutions (SPTR)

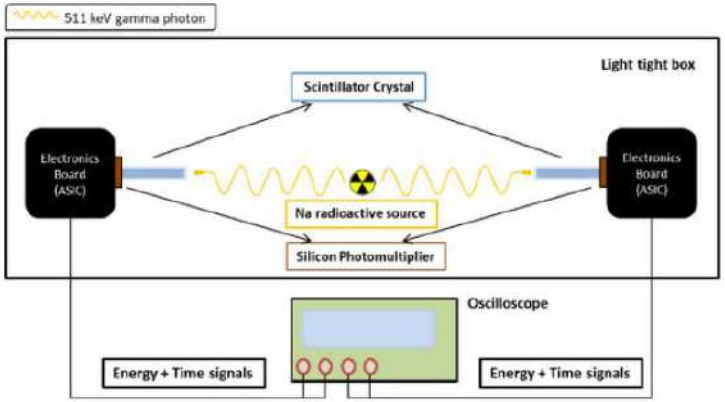


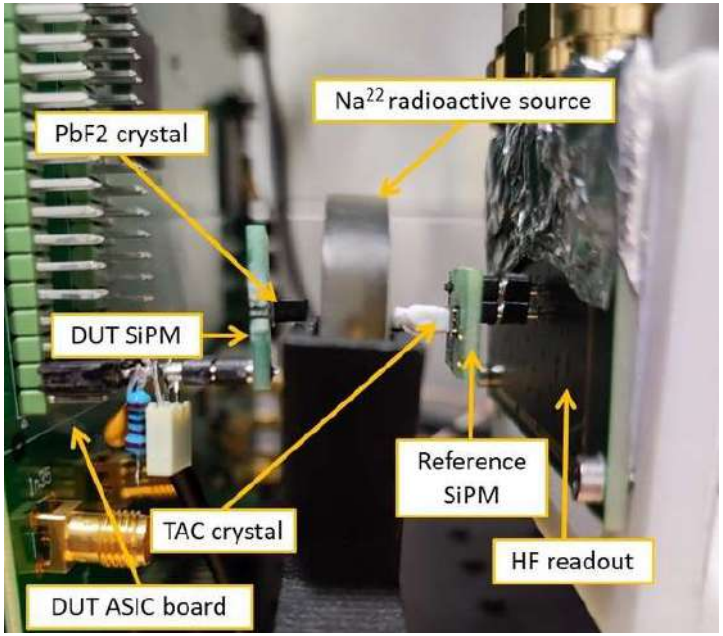


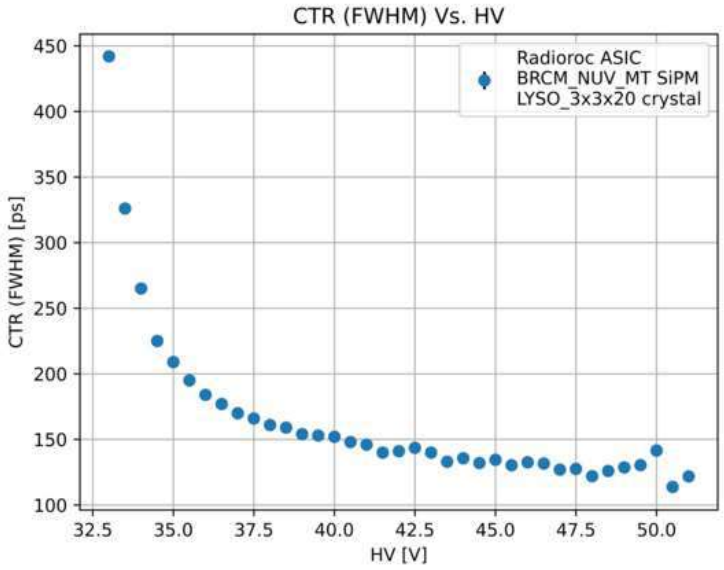


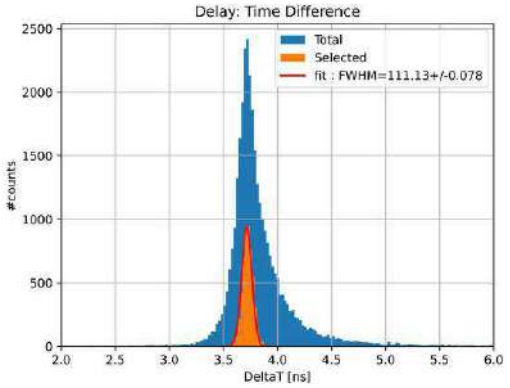
Back to PET

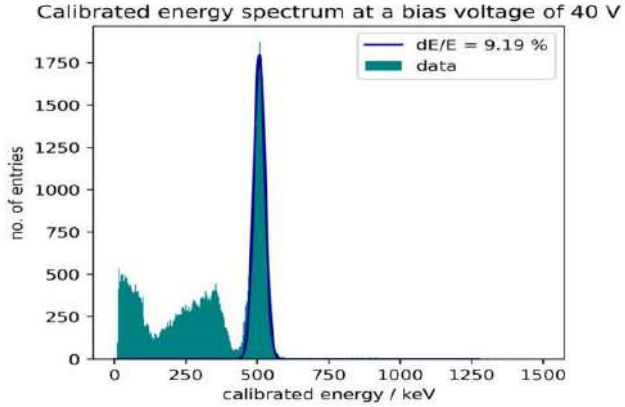
[T. Saleem et al. 2023 JINST **18** P10005]











Summary

- Timing detectors ramping up !
  - Require highly integrated R/O electronics : System On Chip
  - Low power, low noise, high speed…
  - Timing capability down to a few tens of ps
  - Lots of system issues : ck distribution, digital noise, stray inductance…

- Timing performance dominated by sensor characteristics
  - Capacitance, duration, MIP charge
  - Theory predicts :
  - Electronics affects only $g_m \sim Id/2U_T$

$$\sigma_t^{\ J} = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

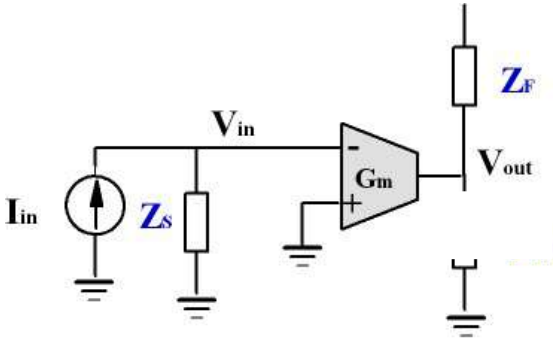
- Joint optimization sensor + readout electronics

Conclusion

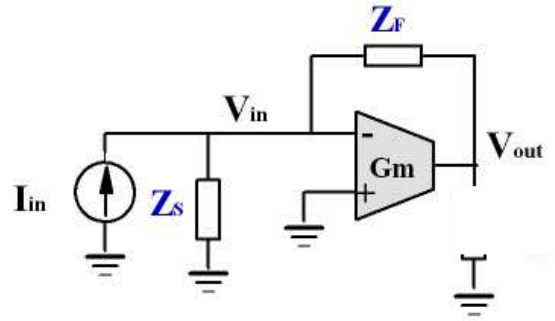
High speed amplifiers

- Response to very short pulse

- Broadband
  - Zin=Rs (50 Ohm)
  - Vin = Q/Cin
  - $\mathbf{V_{OUT} = -G_m R_F \frac{Q_{IN}}{C_d}}$



- Transimpedance
  - Zin ~ Zf/G ~ 1/gm
  - $\mathbf{V_{OUT} = \frac{\frac{1}{G_m} - R_F}{1 + j\omega\frac{C_d}{G_m}} I_{IN} \approx -G_m R_F \frac{Q_{IN}}{C_d}}$

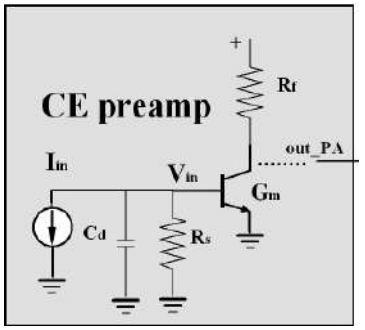


- Same response at High Frequency
- For highest speed : go to broadband. Faster, less stability issues

High speed amplifiers

- Jitter is given by [details in backup] :

$$\sigma_t^J = \frac{N}{dV/dt} = \frac{e_n}{\sqrt{2t_{10-90\_PA}}} \frac{C_d\sqrt{t_{10-90\_PA}^2 + t_d^2}}{Q_{in}} = \frac{e_n C_d}{Q_{in}} \sqrt{\frac{t_{10-90\_PA}^2 + t_d^2}{2t_{10-90\_PA}}}$$



- Optimum value: $t_{10\text{-}90\_PA} = t_d$ (current duration)

$$\sigma_t^J = \frac{e_n C_d}{Q_{in}} \sqrt{t_d}$$

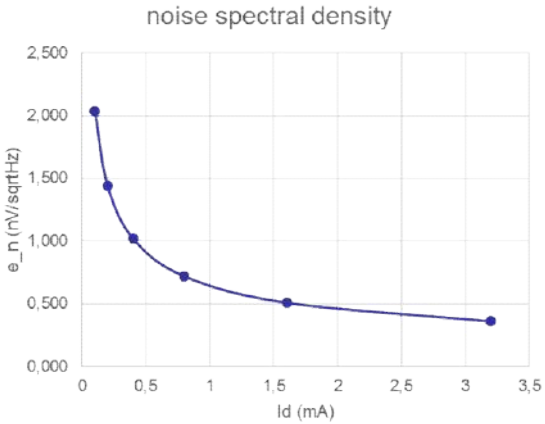
Cd: detector capacitance
$t_{10\_10\_PA}$: rise time of the PA
t_d= drift time of the detector
e_n preamp noise density

Dominated by sensor
Electronics only gives
the spectral density of
the input transistor e_n

- Gives ps/fC as scales with 1/Qin

- Electronics noise e_n given by the input transistor transconductance g_m:

$$e_n = \sqrt{\frac{2kT}{g_m}} \approx \frac{2kT}{\sqrt{qI_D}}$$



Timepix4 : Si pixels with timing [X. Llopart et al. CERN]

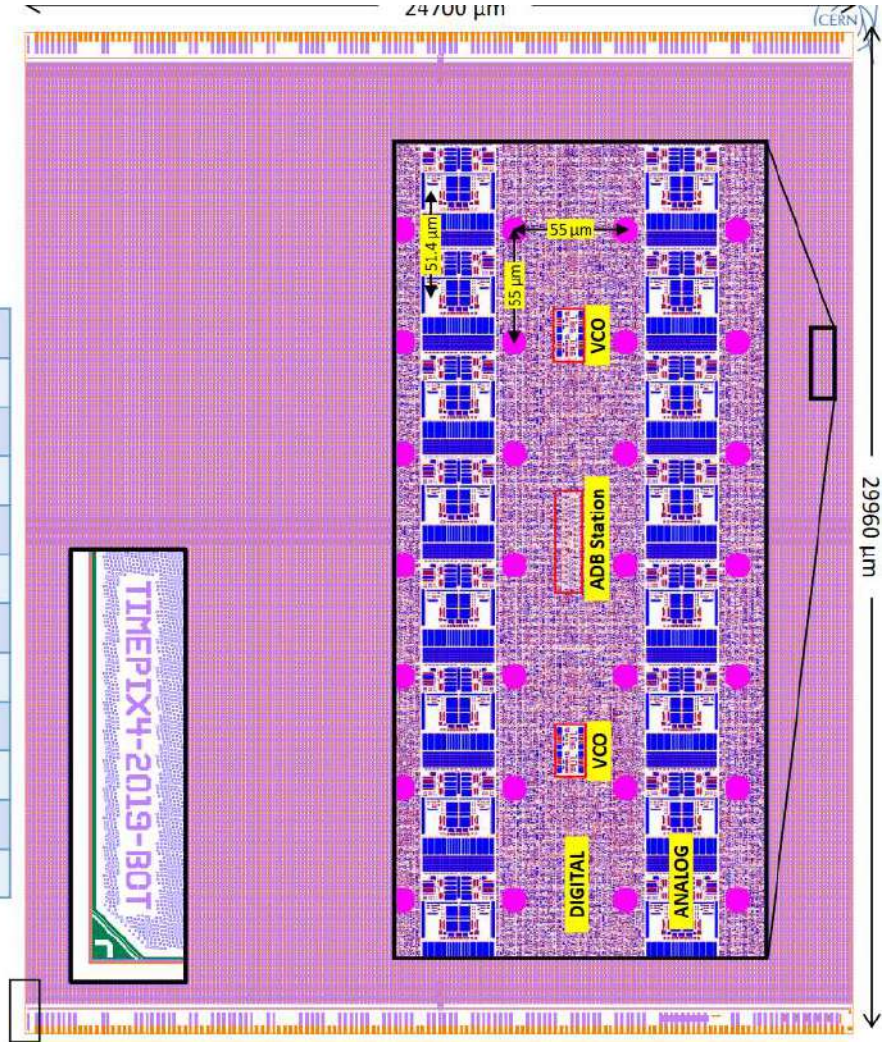
- Si pixels 55x55 µm²
  - CMOS 65nm
  - 230 k pixels
  - ~7 cm² area
  - 4-side buttable
  - 195 ps TDC bins
  - Min threshold ~500 e-

X. Llopart et al. (CERN) https://indico.cern.ch/event/1121147/attachments/2389692/4084909/Xavi_DS_11Feb2022.pdf

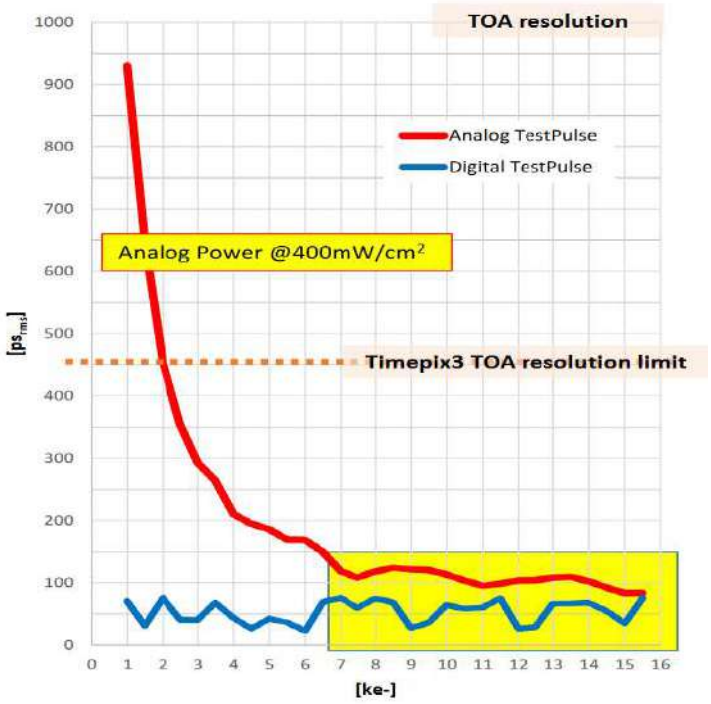
medipix collaboration

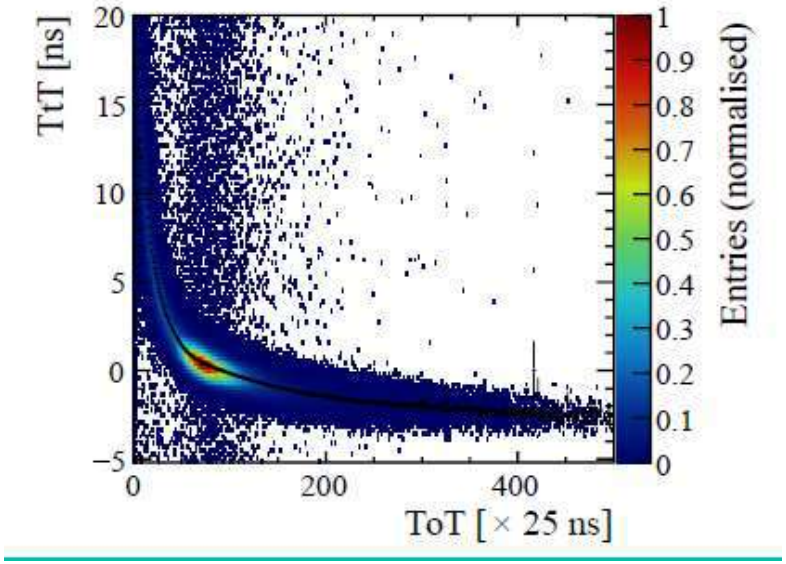
Timepix4 (November 2019)

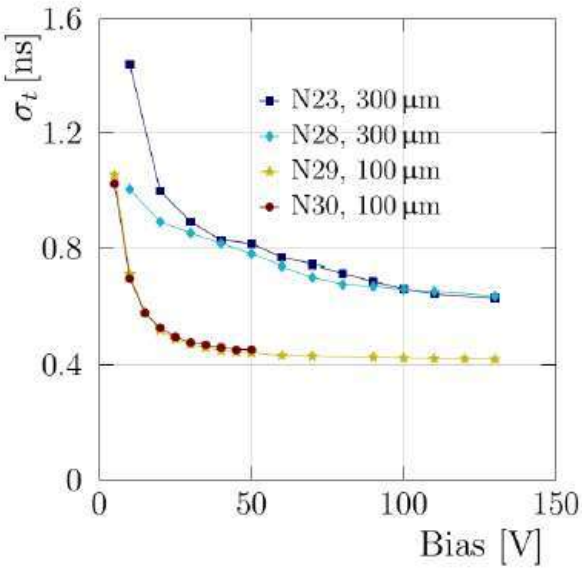
Pixel size	55 x 55 µm
Array	512 x 448
Pixels	229376
aPLL	19
aDLL	16
10.24 Gbps serializers (Nikhef)	16
On-pixel VCO (Nikhef)	28672
dDLL Columns	448
Biasing DACs	13
ADC (IFAE)	1
Transistors in pixel	~6000
Transistors in chip	~1.5 bn



Timepix4 : time resolution

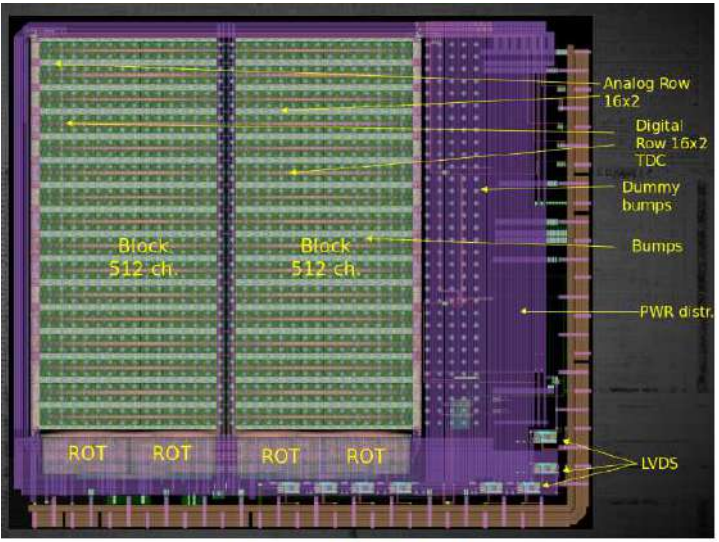




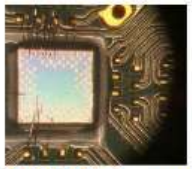


Timespot : Si pixels with timing

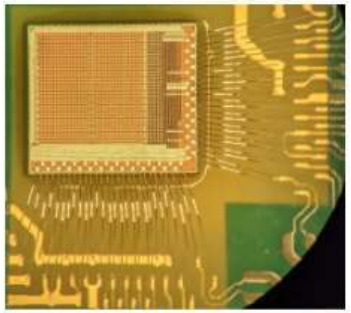
L. Piccolo et al. (INFN) https://indico.cern.ch/event/1019078/contributions/4443945/attachments/2277822/3938469/lorenzo_piccolo_TWEPP2021.pdf



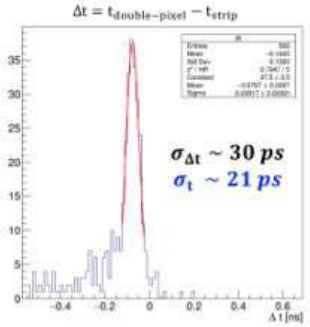
Timespot1 ASIC layout



Timespot0 ASIC (summer 2019) 1.4 mm × 1.4 mm



Timespot1 ASIC (summer 2021) 2.6 mm × 2.3 mm 32×32 pixels



Measured 3D Silicon Sensor performance[1,2].

- Designed in **28 nm CMOS technology**.
- Timespot0 ASIC →
  - Independent blocks test chip, not connectable to the sensor.
  - Resolution ∼ 100 ps.
- The 3D Silicon Sensor has been proven to be a lot more performing than expected → ∼ **20 ps.**
- **Timespot1 ASIC** →
  - **1024 channel matrix, bump-bondable to the sensor.**
  - **Resolution Goal → better than 50 ps** (LHCb-U2 specs).

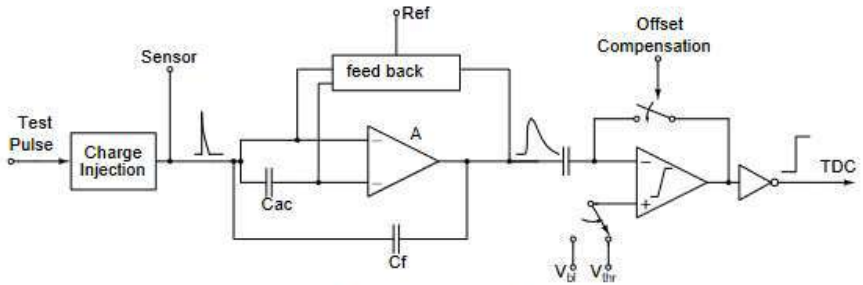
[1] L. Anderlini et al., Intrinsic time resolution of 3D-trench silicon pixels for charged particle detection. Journal of Instrumentation, 15, P09029, 2020.

[2] D. Brundu et al., Accurate modeling of 3D-trench silicon sensor with enhanced timing performance and comparison with beam measurements. arXiv:2106.08191v1 [physics.ins-det], in press on JINST (2021).

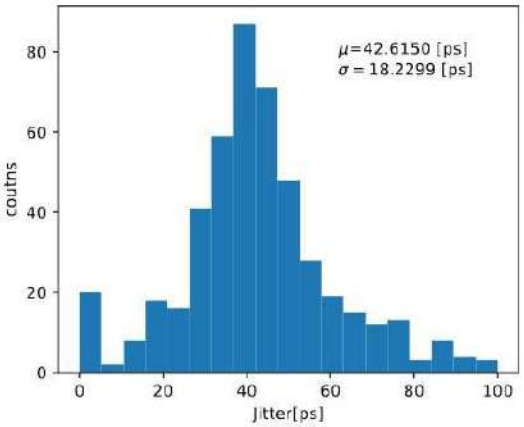
Performance of V1

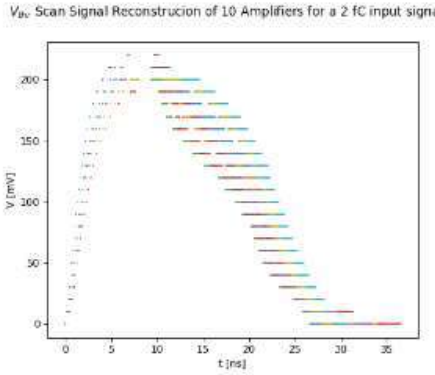
- Jitter : 43 ps rms
  - 2 fC injected = 1 MIP
  - Already good…
  - But expected 30 ps !

Analog FE Tests

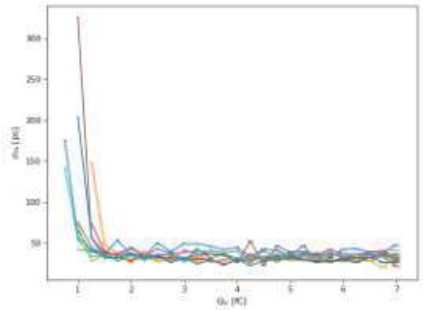


Analog Front-End Schematic





Example of 10-channel Threshold-Scan Signal Reconstruction

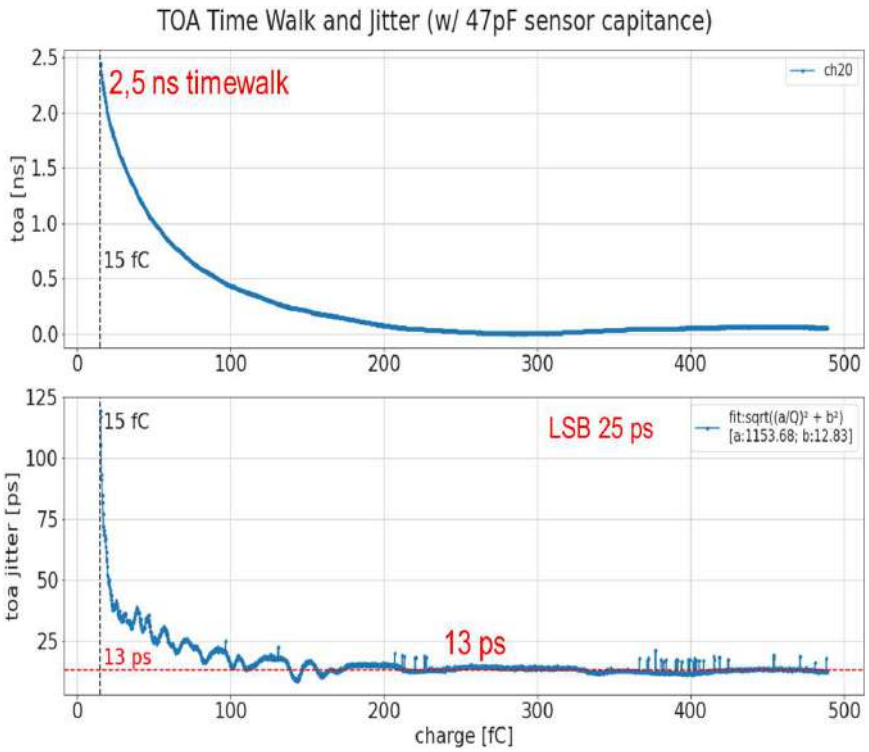


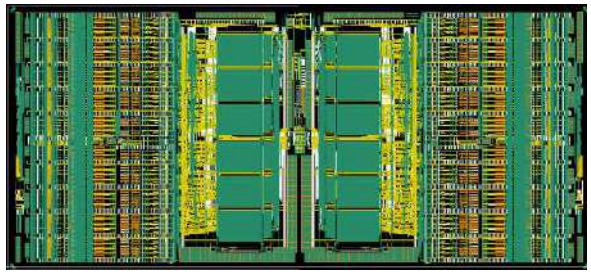
Example of 10-channel jitter VS input charge trend

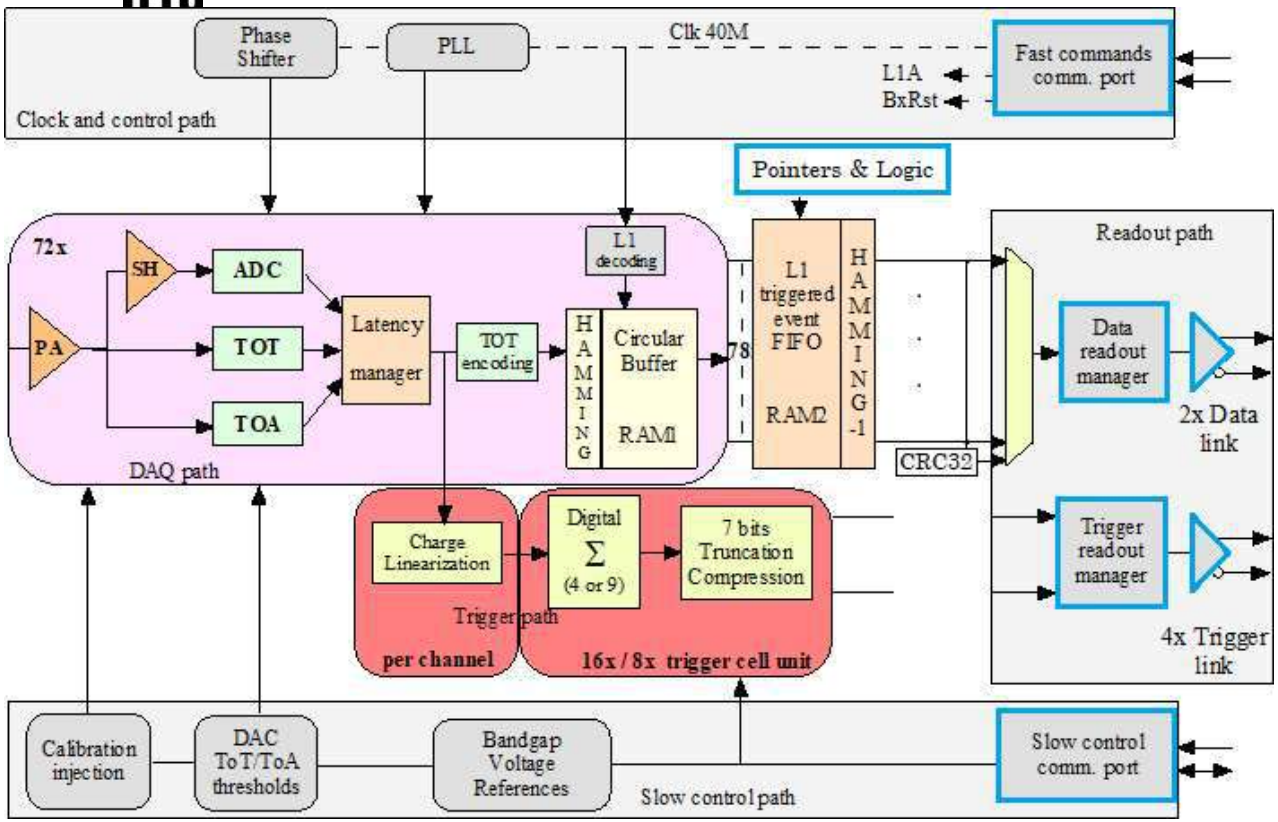
- Pulsed using the **per-pixel charge injection capacitance** → input charge (0 → 7 fC).
- The signal is injected with the next **reference clock rising-edge** → time-0 measurment.
- Discriminator **Baseline and Threshold set** via 2 independent voltages.
- **Output → Discriminator-only** → CSA signal must be reconstructed.

Si readout : HGCROC

- CMS HGCAL readout ~1 cm² Si pads (50 pF)
  - 72 channels calorimeter/timing readout
  - Also a SiPM variant







HGCROC3 performance