Compact Low-Power mm-wave ICs for Next-Generation (5G/6G) Wireless Transceivers

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Outline

- Ultra-Scaled Silicon Technologies
  - Impact of passive losses in low-power mm-wave ICs
- Low-Power Compact mm-wave ICs for 5G/6G Phased-Array Transceivers
  - Variable-Gain Low Noise Amplifier
  - Benchmarking and validation (rvt vs. slvt)
- Conclusions

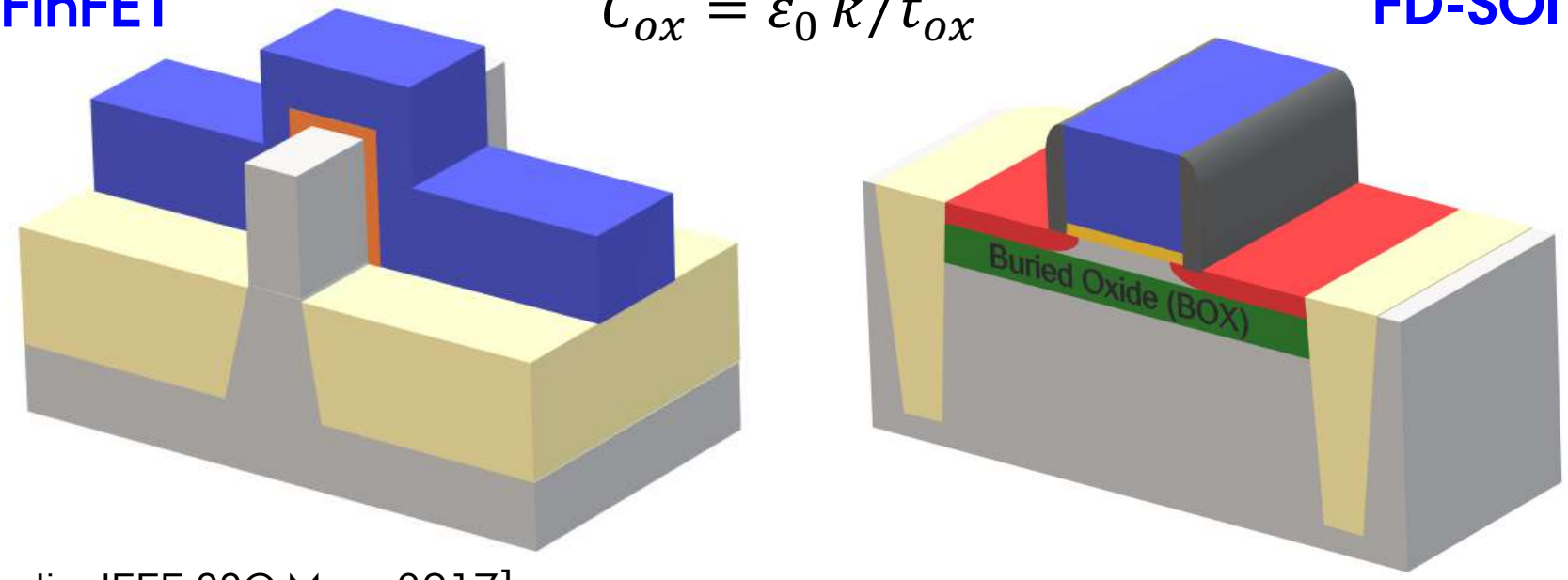
Si Tech Evo: CMOS Techs

- Ultra-scaled device evolution driven by **charge control improvement** and **leakage current reduction**
- Two fully depleted (FD) techs emerged with **22/28nm** CMOS node (double patterned, high-k dielectrics, metal gate, strained Silicon)

FinFET

$$C_{ox} = \varepsilon_0 \, k / t_{ox}$$

FD-SOI



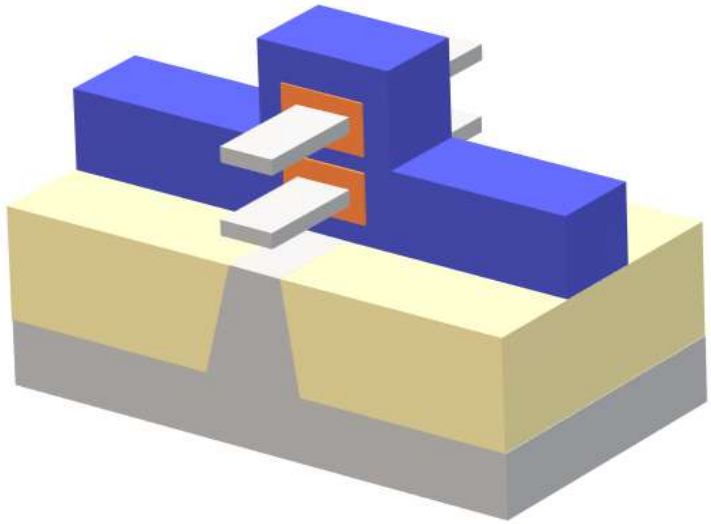
[Cathelin, IEEE SSC Mag. 2017]

[Zito, IEEE ISC 2019]

Si Tech Evo: The “Last” CMOS Transistors

- **Samsung** has introduced a different transistor design starting from the **3nm** node

- The next transistor has already many names
  - **gate-all-around**
  - **multi-bridge channel**
  - **nano-beam**
  - **nano-sheet**



[Ye, Ernst, Khare, IEEE Spectrum, Jul. 2019]

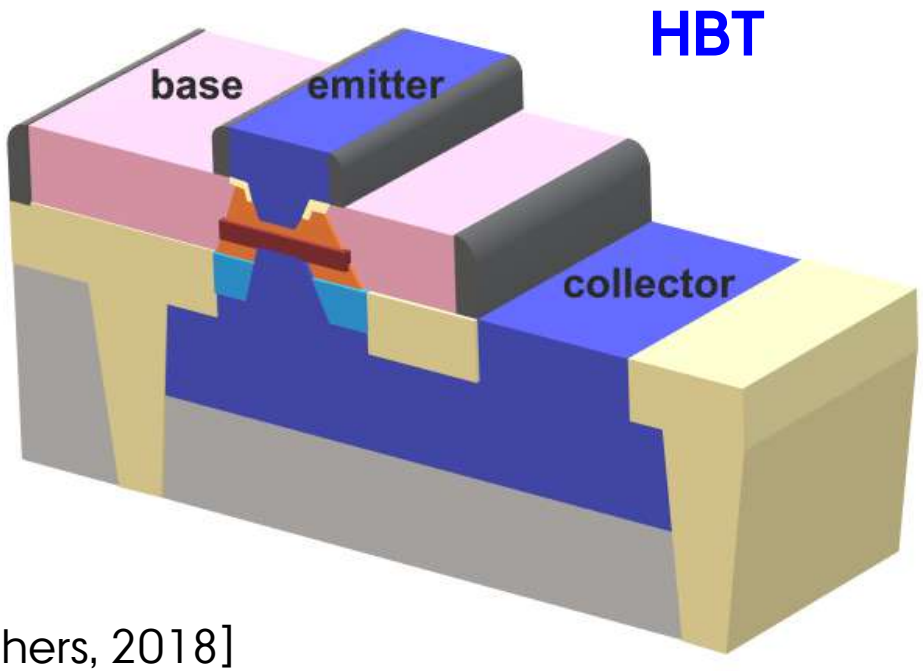
Si Tech Evo: SiGe BiCMOS Techs

- Device evolution driven by **higher frequency operations** (f_T, f_{max}) and **integration with scaled CMOS devices**
- High-speed SiGe/SiGe:C Heterojunction Bipolar Transistors (HBTs) together with high-density CMOS

- $f_{max} \approx \sqrt{\frac{f_T}{8\pi R_B C_{BC}}}$

R_B: base resistance

C_{BC}: base-collector capacitance

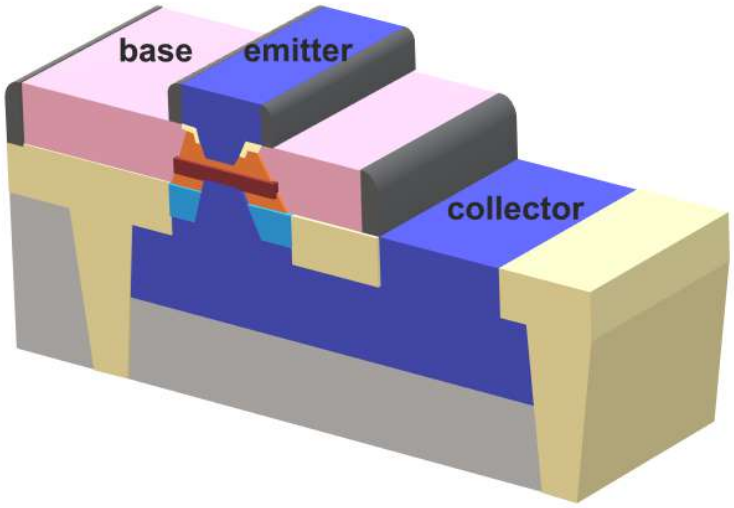


[Rücker, Heinemann, Ch. 1, River Publishers, 2018]

Si Tech Evo: SiGe BiCMOS Advantages

- **HBT** f_T less sensitive to parasitic capacitance of metal layers
- More mature **back-end-of-line (BEOL)**, leading to better passives
- Lower **costs**

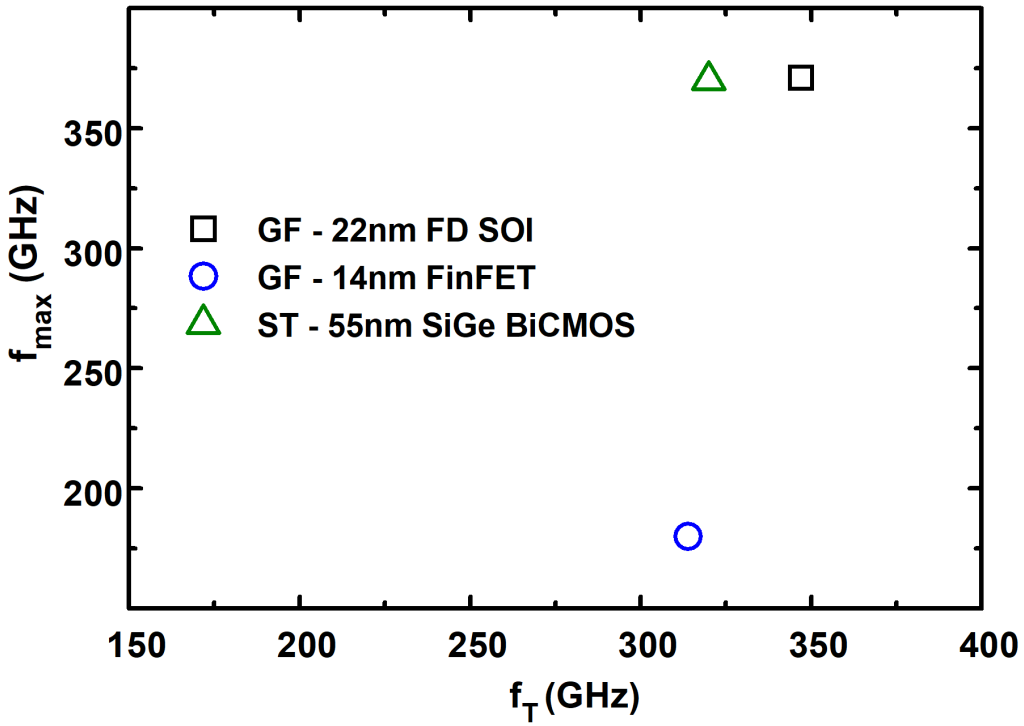
HBT



[Chevalier et al. IEEE BCICTS 2018]

Si Tech Evo: FoMs

- **FinFET**, **FD-SOI** and **HBT** devices commercially available
  - f_T > 300 GHz
  - f_{max} > 150 GHz



- **Active devices** have **outstanding performances** with **great potential for high-frequency applications**

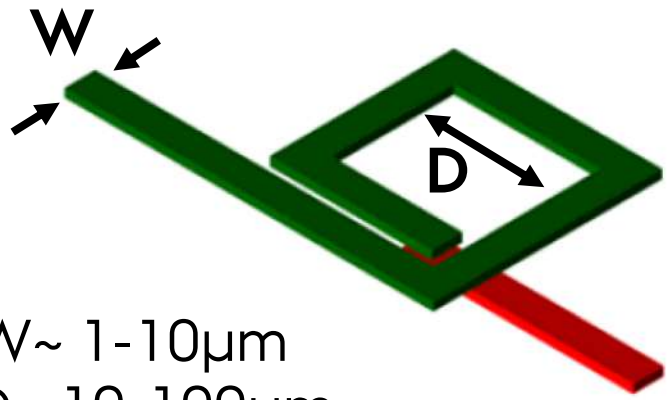
[Ong et al. IEEE RFIC 2018]
[Chevalier et al. IEEE IEDM 2014]

Si Tech Evo: mm-wave Applications

- **These outstanding performances are enabling a plethora of applications**
  - **High data-rate communications for next generation wireless networks (5G and beyond)**
  - High-speed wireline communications
  - Autonomous and near-autonomous vehicles
  - Virtual reality
  - Radio astronomy
  - Earth observations
  - Satellite communications
  - **Quantum computing**

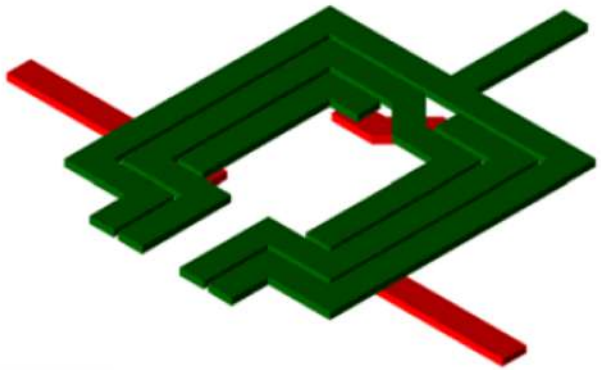
Si Tech Evo: Inductors, Transformers, TX Lines

Inductor



W~ 1-10µm
D ~10-100µm
@60 GHz
L ~ 50-500pH
Q ~ 25-5

Transformer



Co-planar waveguide

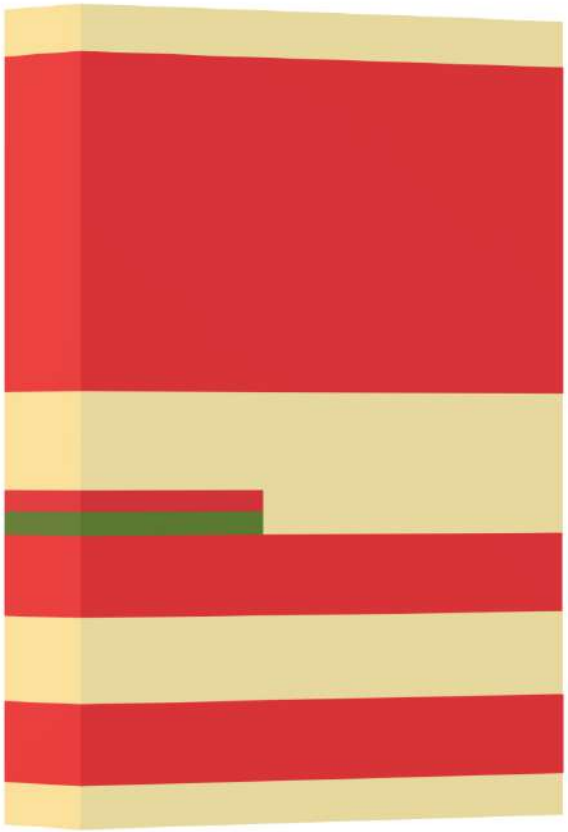
[Pepe, et al. ISSC 2016]

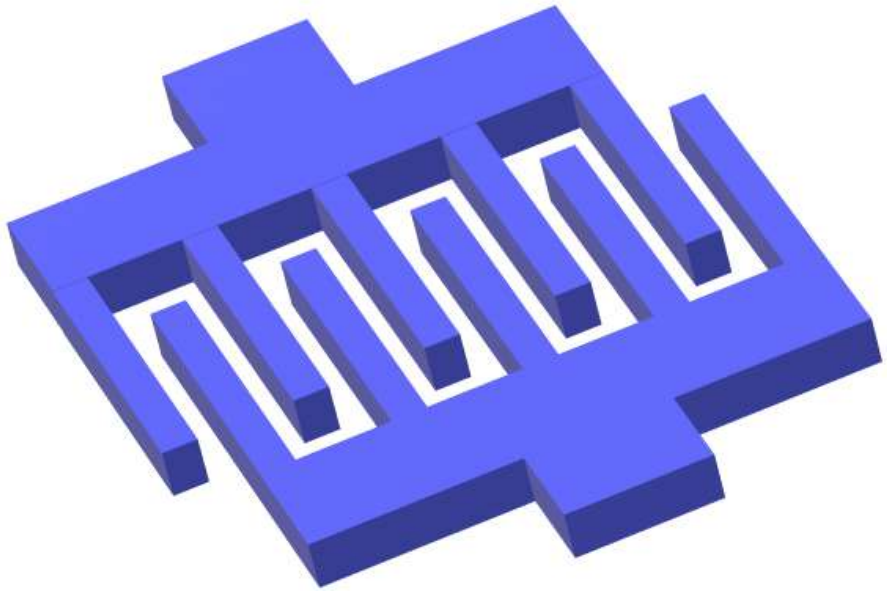
Si Tech Evo: Capacitors

MIM

MOM

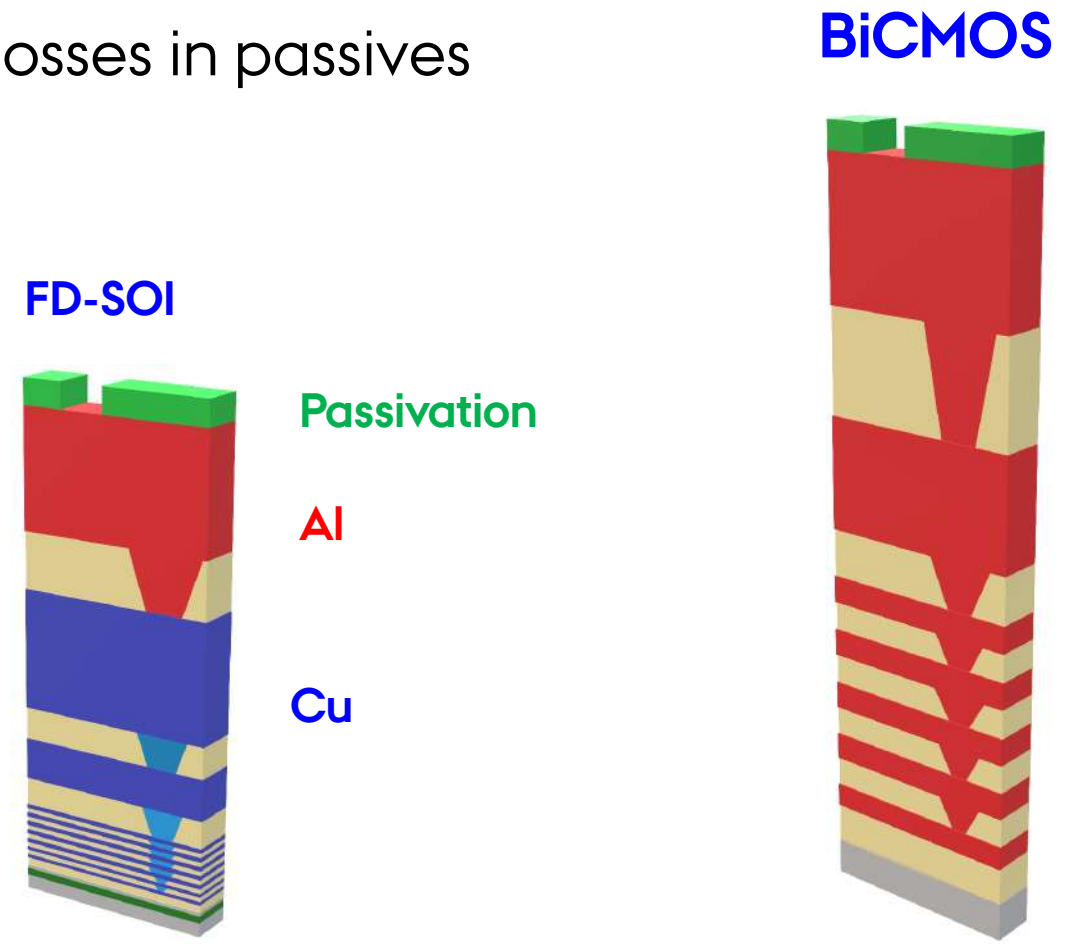
Metal
Insulator
Metal





Si Tech Evo: Back-End-Of-Line (BEOL)

- The impact of losses in passives

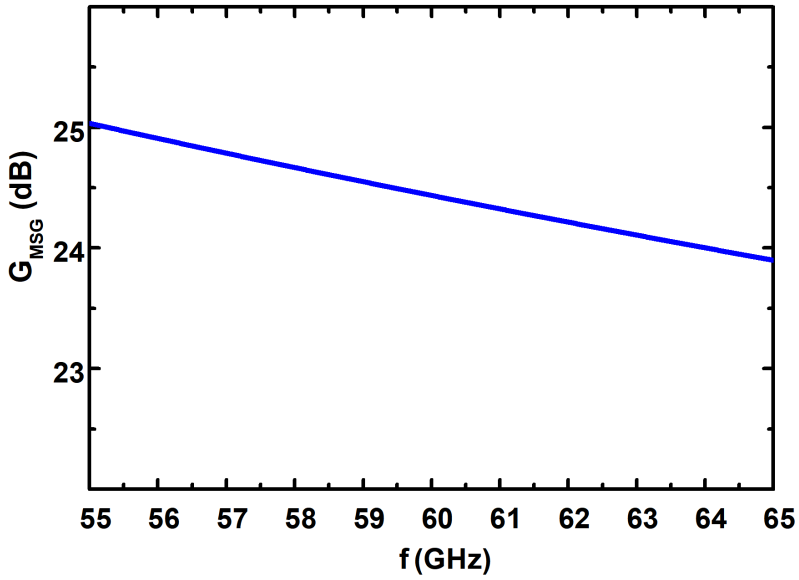


Losses have a dramatic impact on performance ⇨ up to 100%

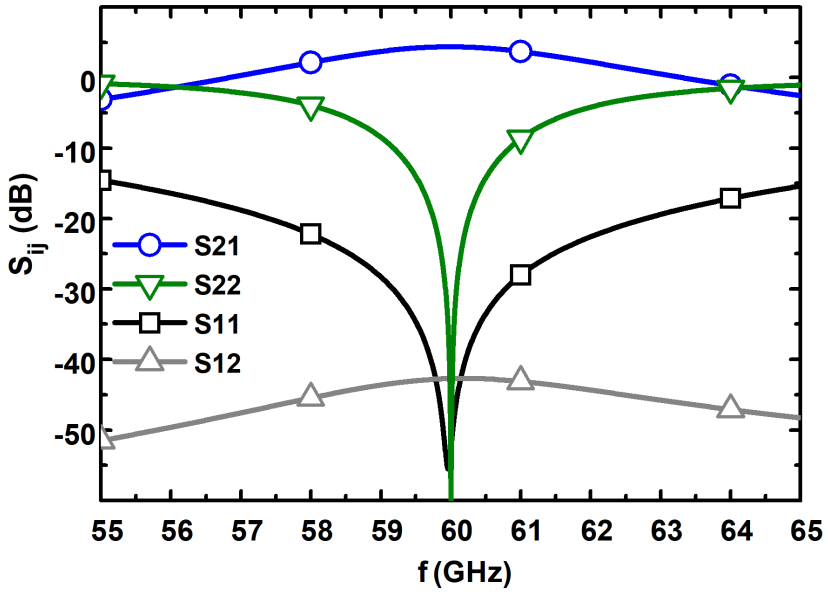
[Zito et al. IEEE ISC 2019]

Impact of Losses: Traditional Loss-Less Design Methodology

AN maximum stable gain



LNA S-parameters

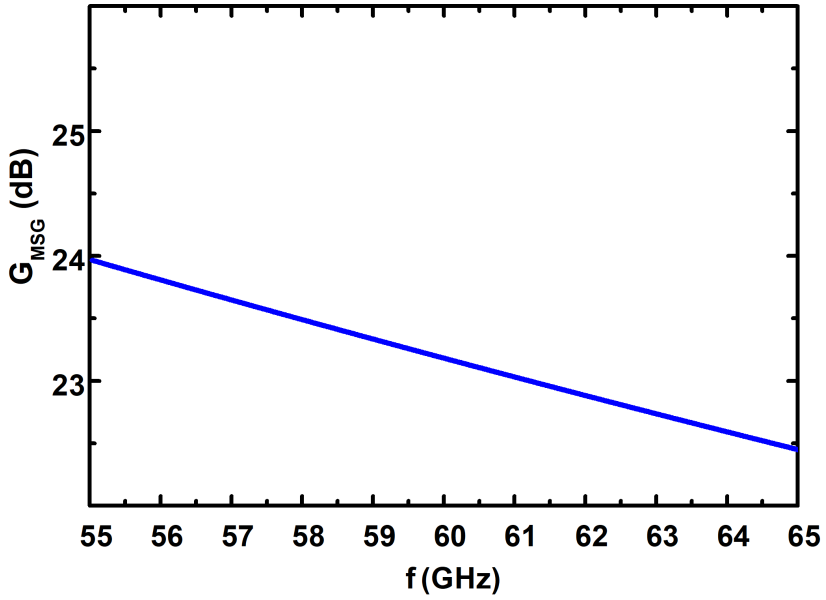


- Despite AN maximum stable gain $\left(G_{MSG}^{AN}\right)$ of **24.4 dB**, MN losses reduce S_{21} to **4.4 dB** !
- **Losses spoil transistor gain potential**

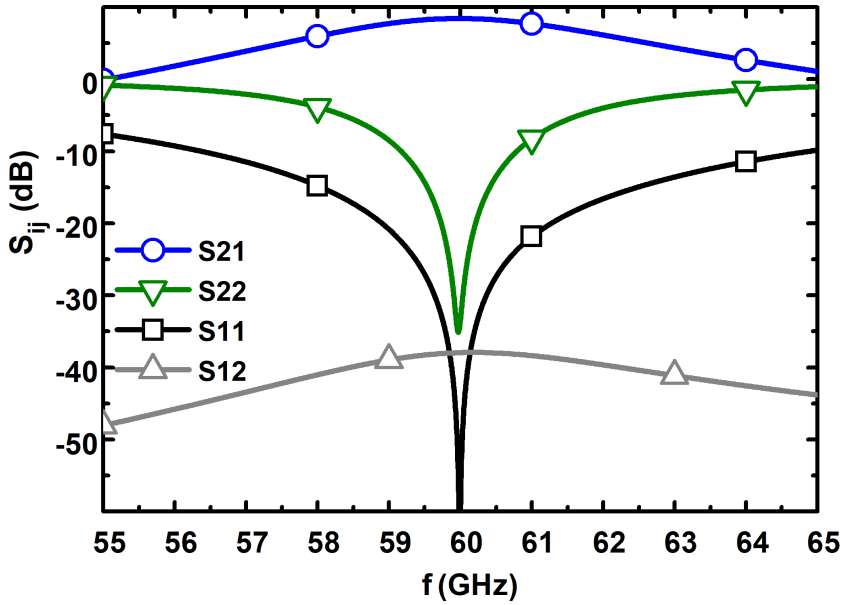
[Zito et al. IEEE ISC 2019]

Impact of losses: advanced loss-aware design methodology

AN maximum stable gain



LNA S-parameters



- Despite AN maximum stable gain $\left(G_{MSG}^{AN}\right)$ of **23.2 dB**, MN losses reduce S_{21} to **8.4 dB**
- **The loss-aware methodology reduces the impact of losses**

[Zito et al. IEEE ISC 2019]

Takeaways (1/2)

- The evolution of silicon technologies has led to transistors with excellent performance for operation at mm-waves
- However, losses in passive devices impede the full exploitation of transistors potential for low-power mm-wave ICs
- Our case study on mm-wave LNA design unveils (quantitatively) the dramatic performance degradation due to MN losses and the benefits of loss-aware design strategies

[Zito et al. IEEE ISC 2019]

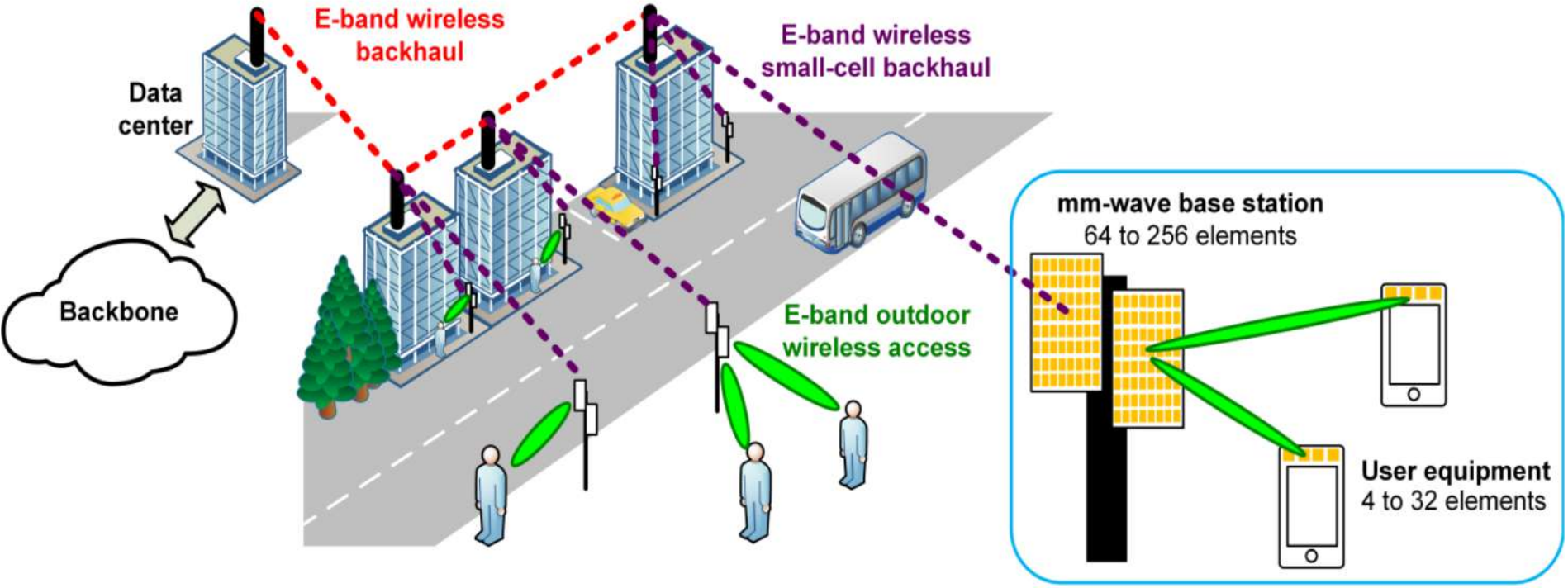
Takeaways (2/2)

- The results indicate the strong **need of further technology advances towards better passives**
  - new materials
  - new technology processes
- Also, **loss-aware design methodologies are a must** and key to design ICs and systems **in the mm-wave frequency range and beyond – especially for low-power ICs**

[Zito et al. IEEE ISC 2019]

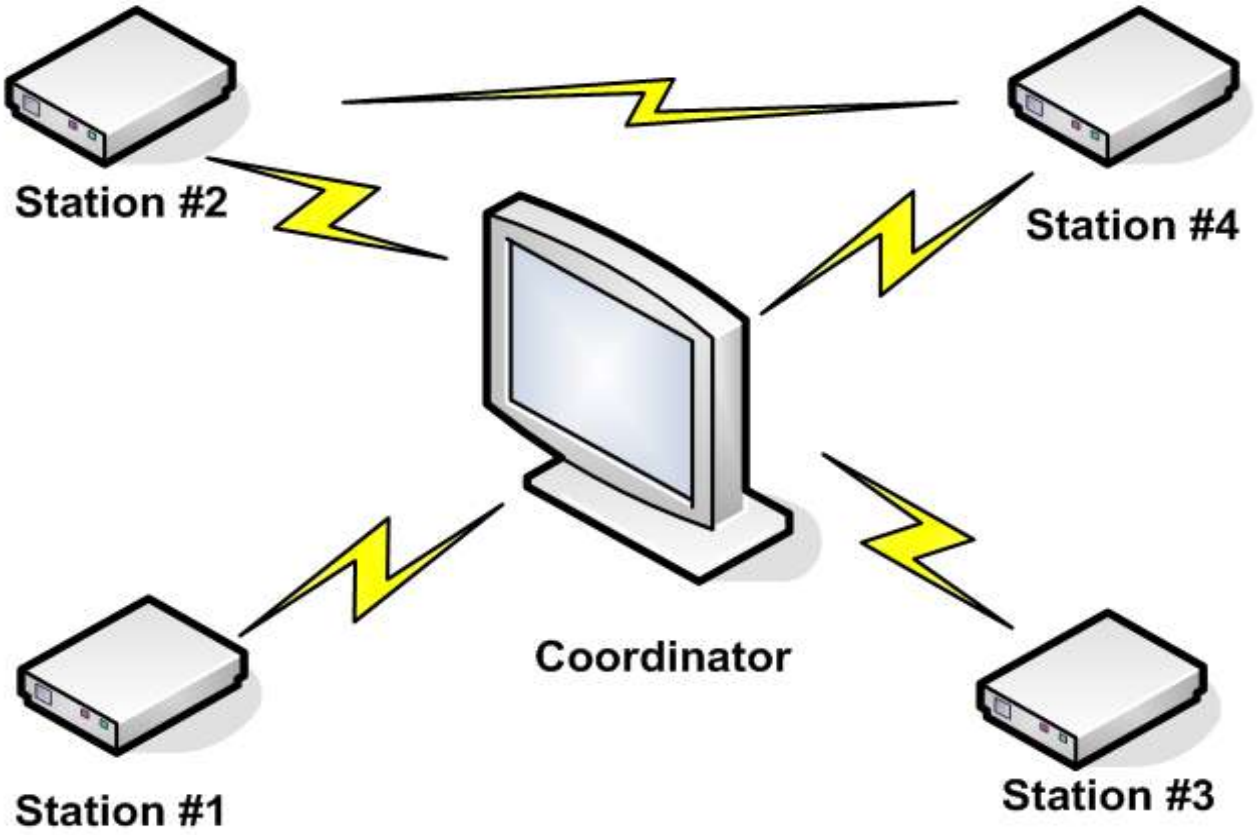
Next-Generation (5G & beyond) Wireless Comms

- E-Band *point-to-point* & *point-to-multi-point* Wireless Local Area Networks & Broadband Internet Access
  - Massive MIMO Systems
  - Data Centers (Clouds)



Next-Generation (5G & beyond) Wireless Comms

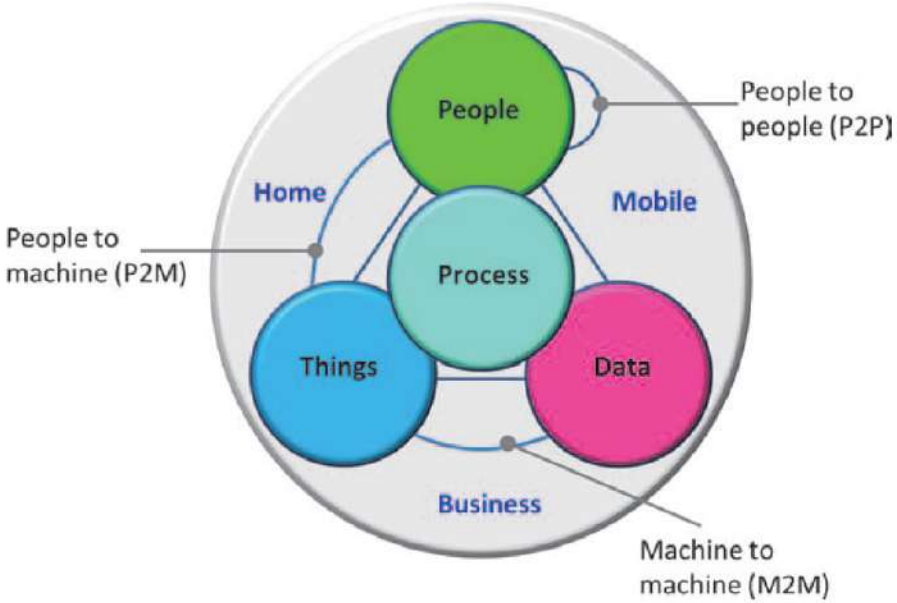
- 60 GHz Uncompressed Wireless HD Video Area Networks
  - 2.5 Gb/s

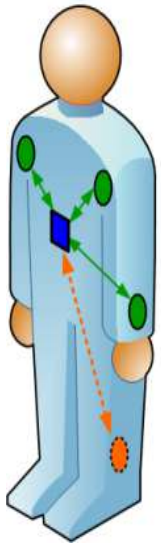


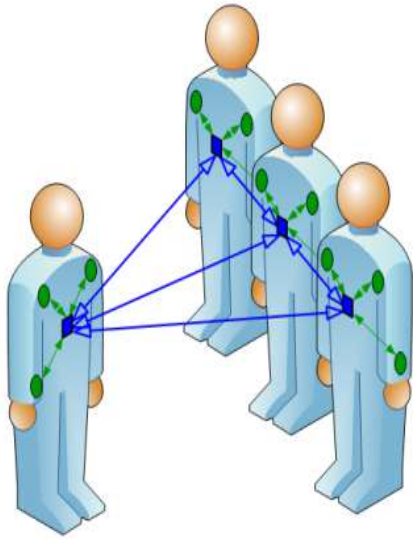
[Pepe et al. IEEE ICECS 2010]

Next-Generation (5G & beyond) Wireless Comms

- Internet of Things (IoT) - Internet of Everything!
  - P2P, P2M and M2M communications & contactless sensing
  - 60 GHz On- & Off-body communications





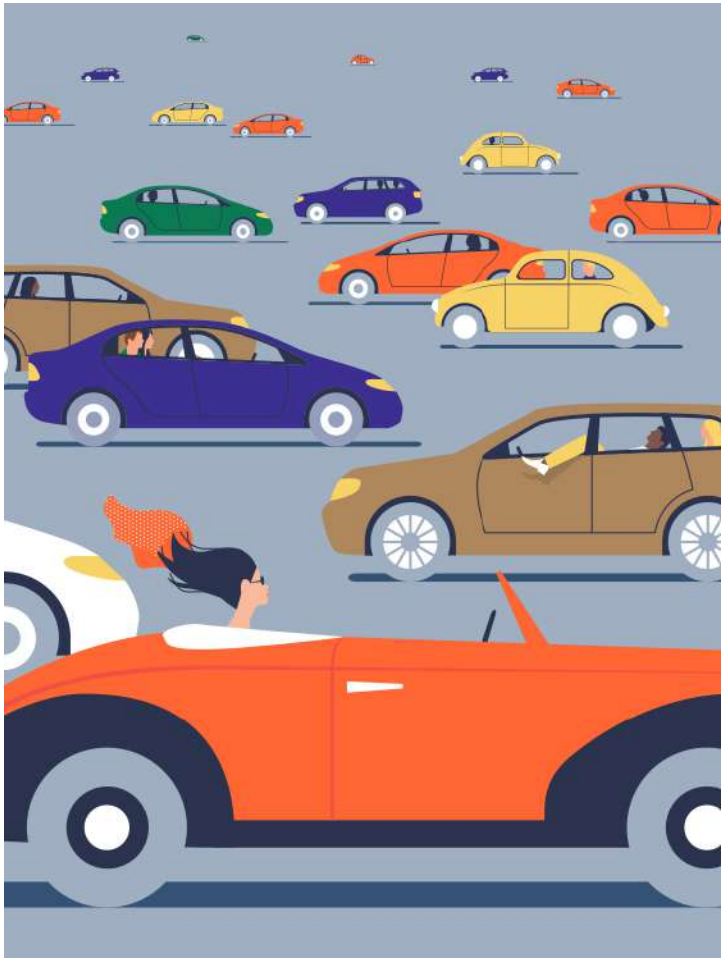


[Zito et al. Springer 2014]

Next-Generation (5G and Beyond) Wireless Comms

- E-Walls, e-Cars (autonomous/driverless vehicles)

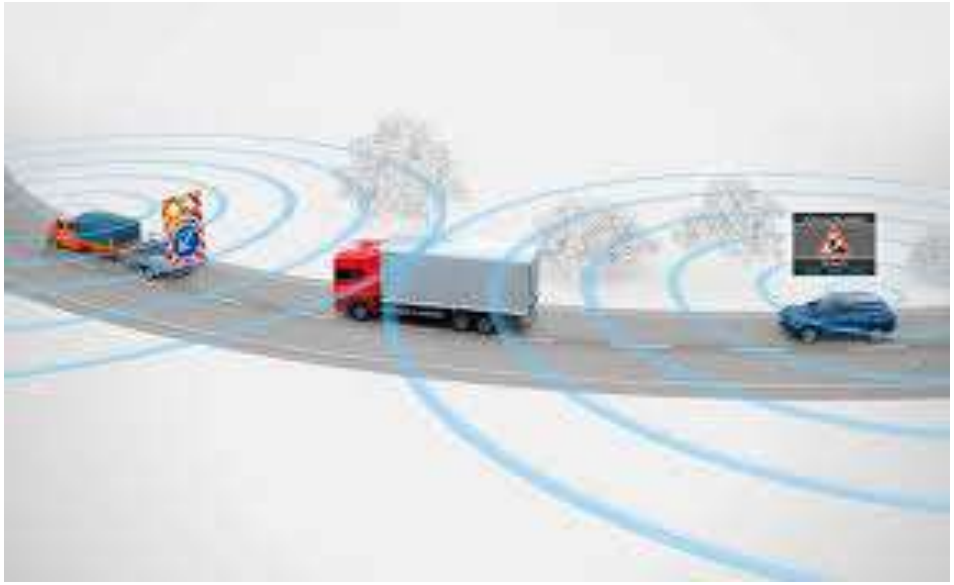
(Source: IEEE Spectrum)



(Source: IEEE Spectrum)

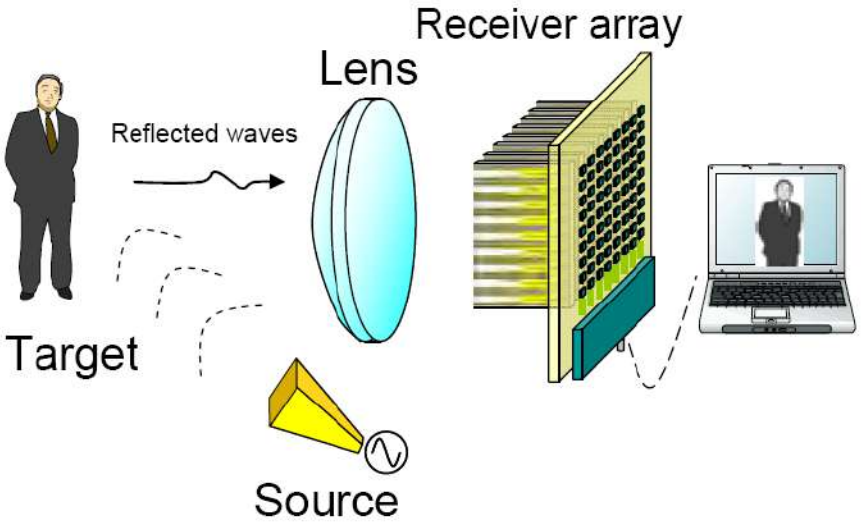
Next-Generation (5G & beyond) Wireless Comms

- Complex (Cyber-Physical) Autonomous Systems
  - Autonomous and near-autonomous vehicles
- Collision-avoidance automotive radars
- Vehicle-to-Vehicle and Vehicle-to-All Communications

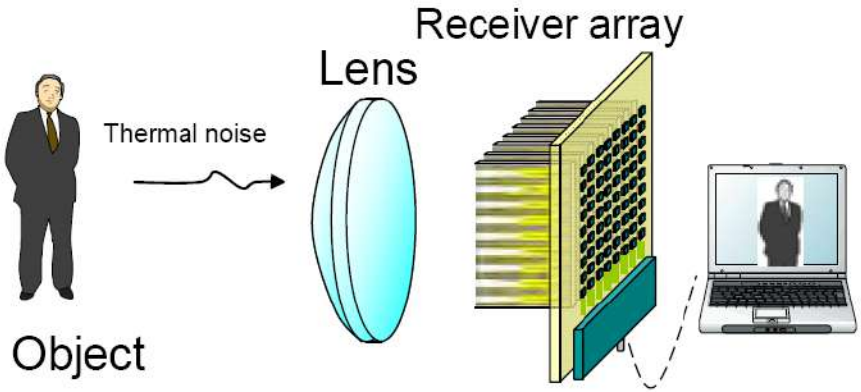


Next-Generation (5G & beyond) Wireless Comms

- Active & Passive Imagers



(a) Active imaging sensor



(b) Passive imaging sensor

[Mereni et al. AICSP. Springer, 2013]

Next-Generation (5G & beyond) Wireless Comms

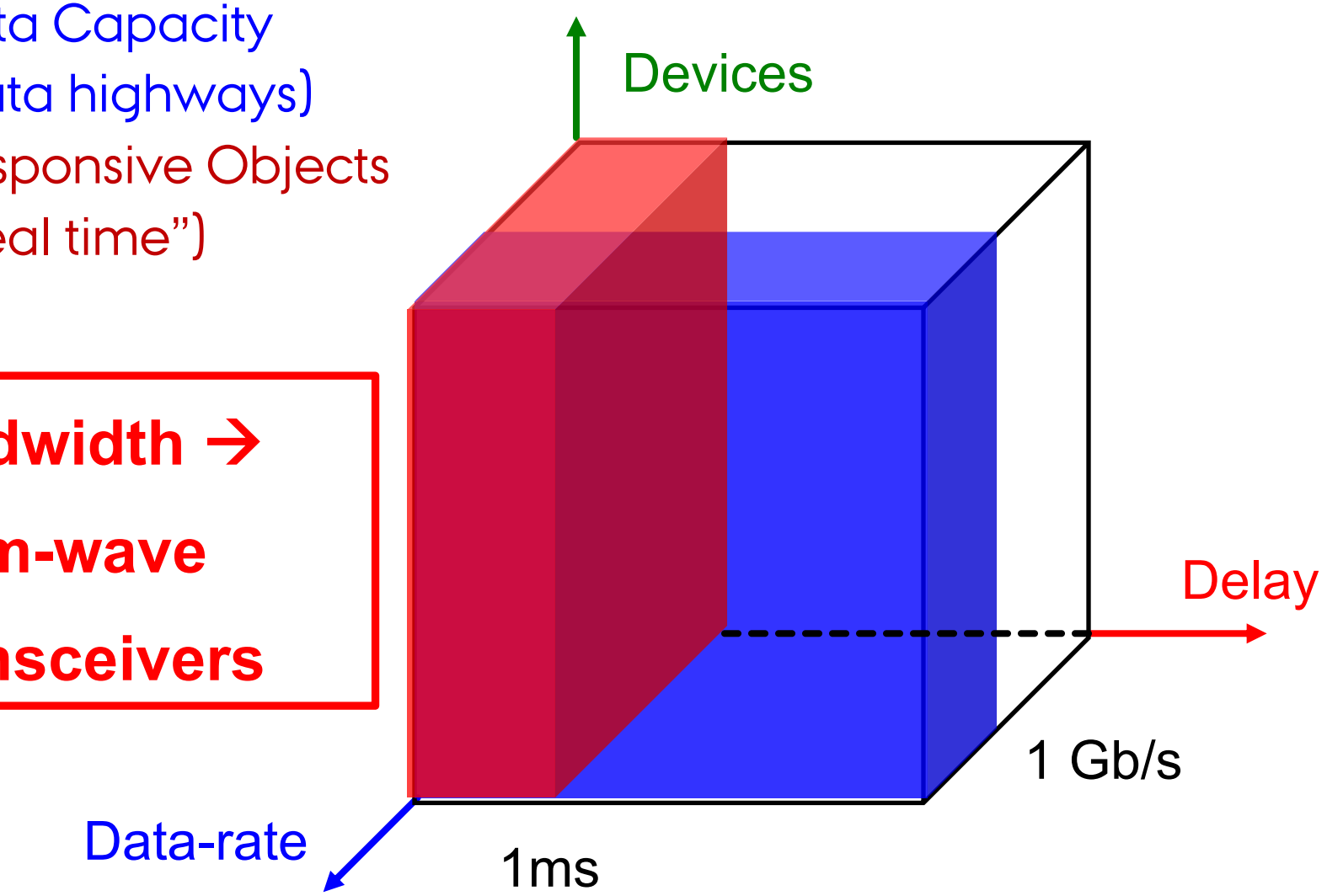
- Expected by 2020
  - Massive growth in data traffic volume (×1000)
  - Massive growth in connected devices (25 Billion devices)
- Key drivers for the development of 5G
  - Low latency (< 1ms)
  - High throughput (>1Gb/s)

[Rappaport et al. IEEE Access 2013]
[Koverman. IEEE Consumer Elec. Mag. 2016]

Next-Generation (5G) Wireless Comms

- 3D (Data-rate, Delay, Devices)
  - Data Capacity (data highways)
  - Responsive Objects ("real time")

Bandwidth → mm-wave Transceivers



Next-Generation (5G & beyond) Wireless Comms

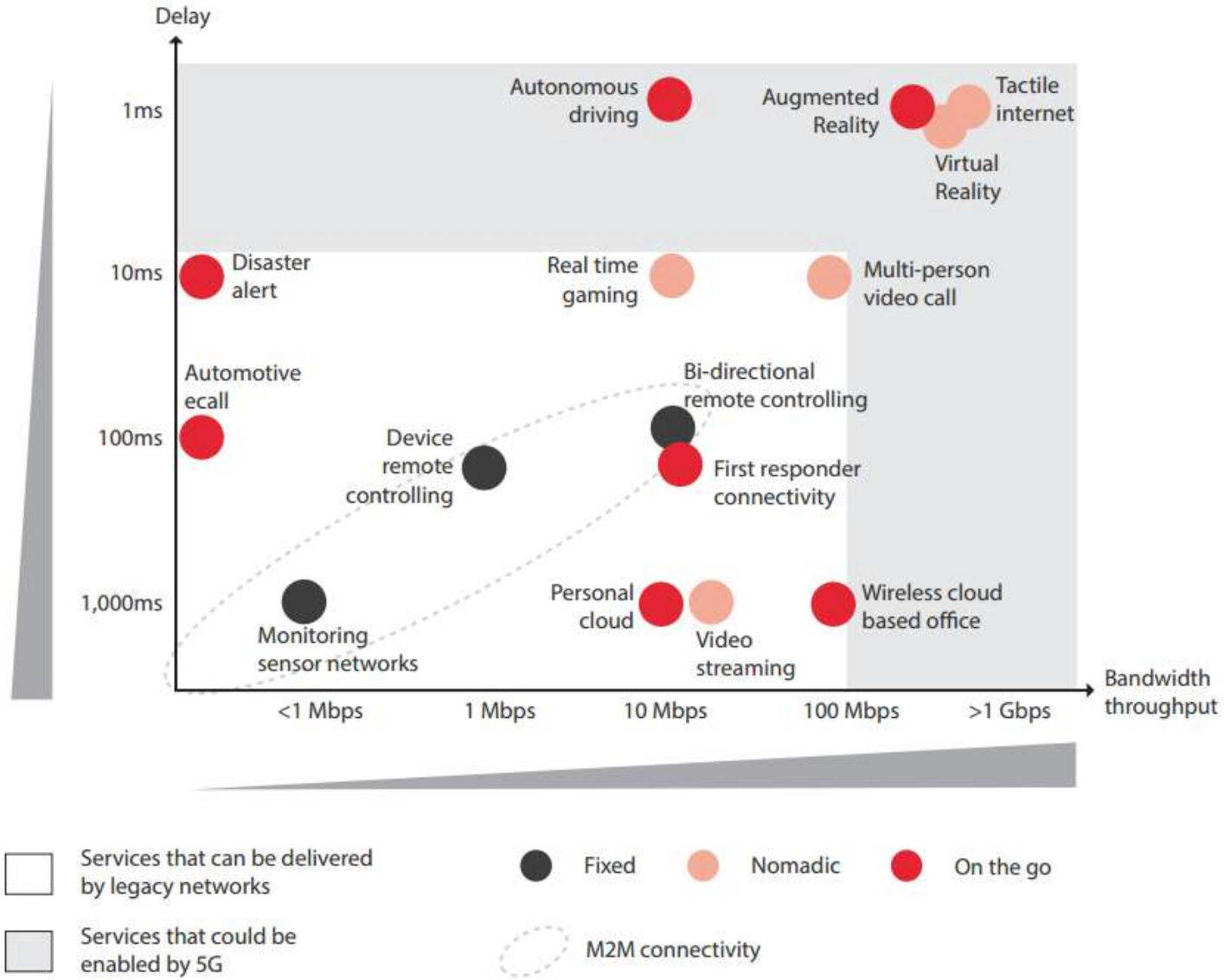
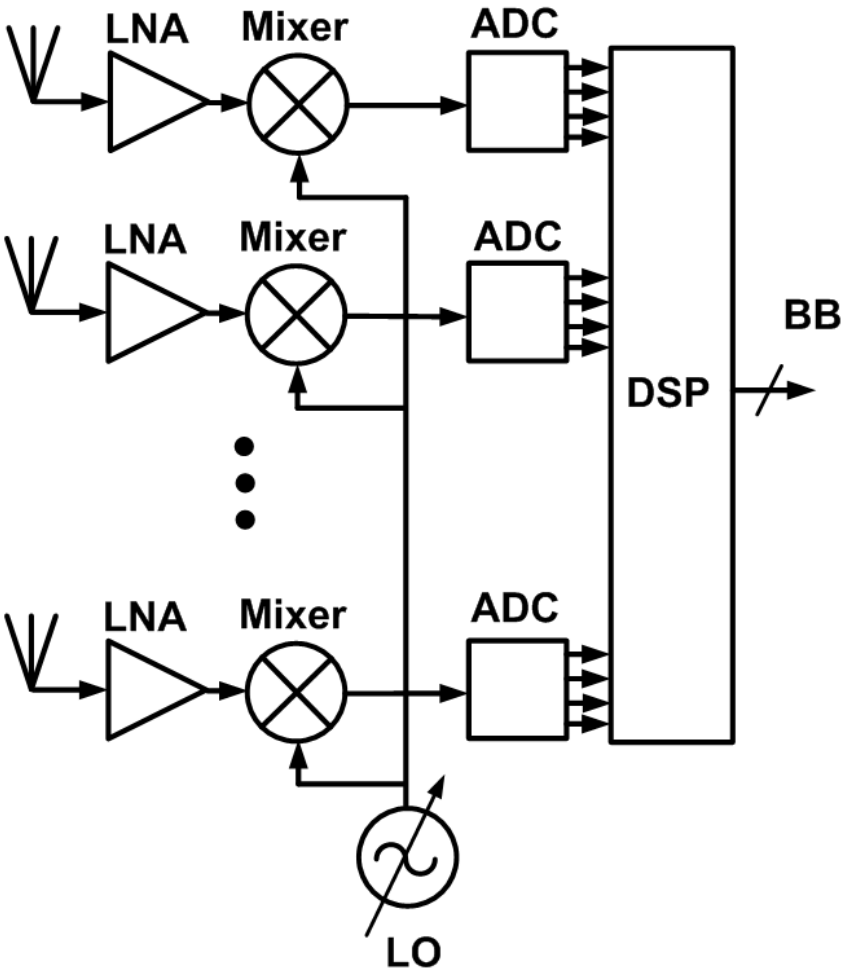


Figure 1: Bandwidth and latency requirements of potential 5G use cases

Source: GSMA Intelligence

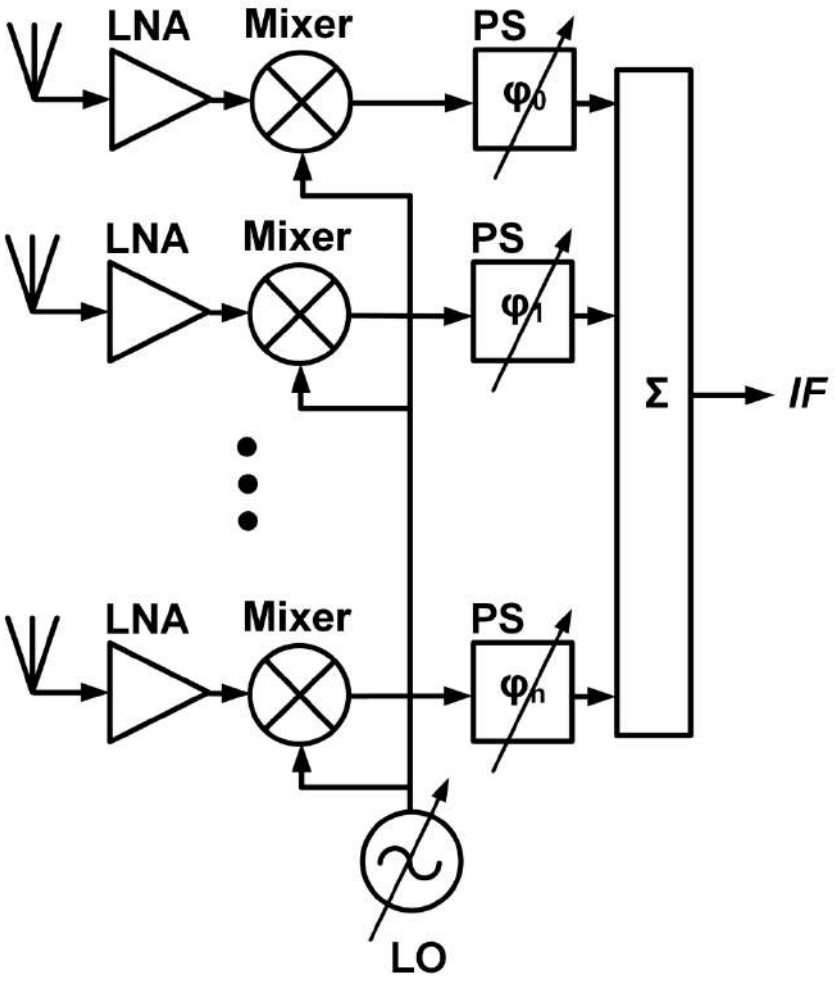
Phase-Array mm-Wave Transceivers

- Phased-Array Architectures
  - Digital (BB) phase shifting
  - True MIMO



Phase-Array mm-Wave Transceivers

- Phased-Array Architectures
  - IF phase shifting
  - "Pseudo" MIMO (MISO)



Phase-Array mm-Wave Transceivers

- Phased-Array Architectures
  - LO phase shifting
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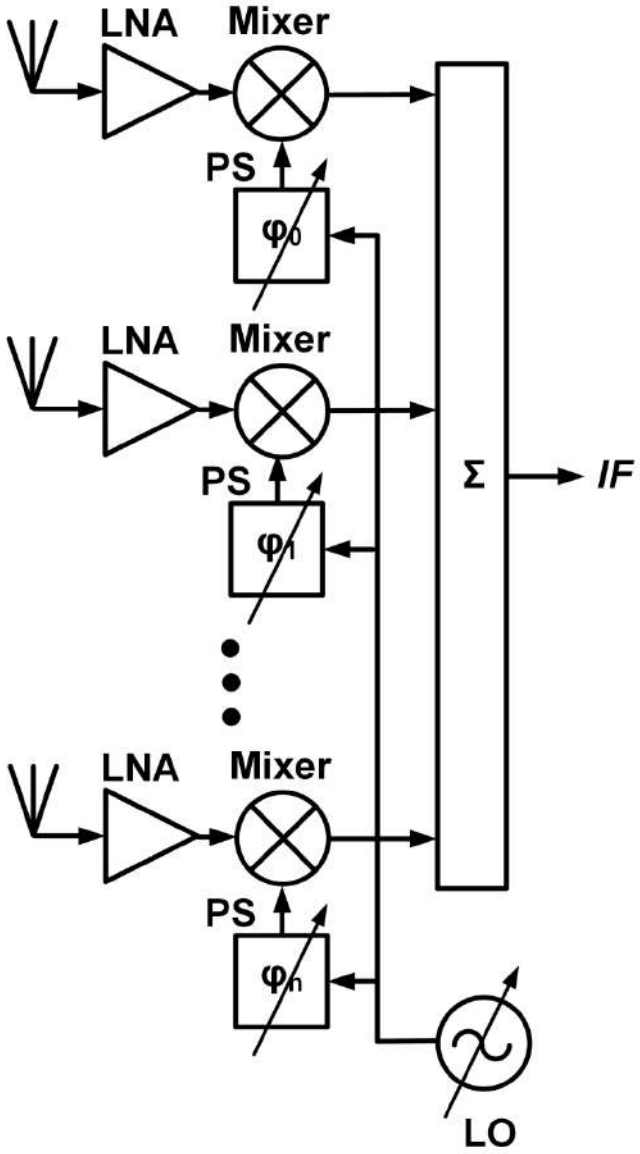
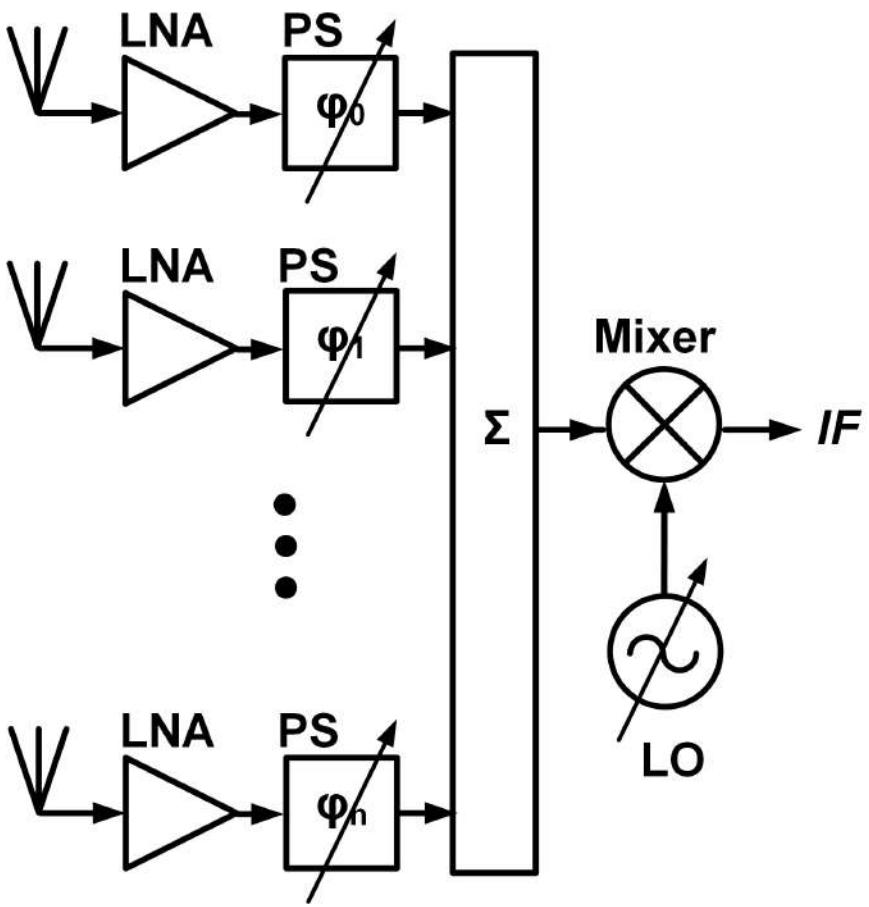


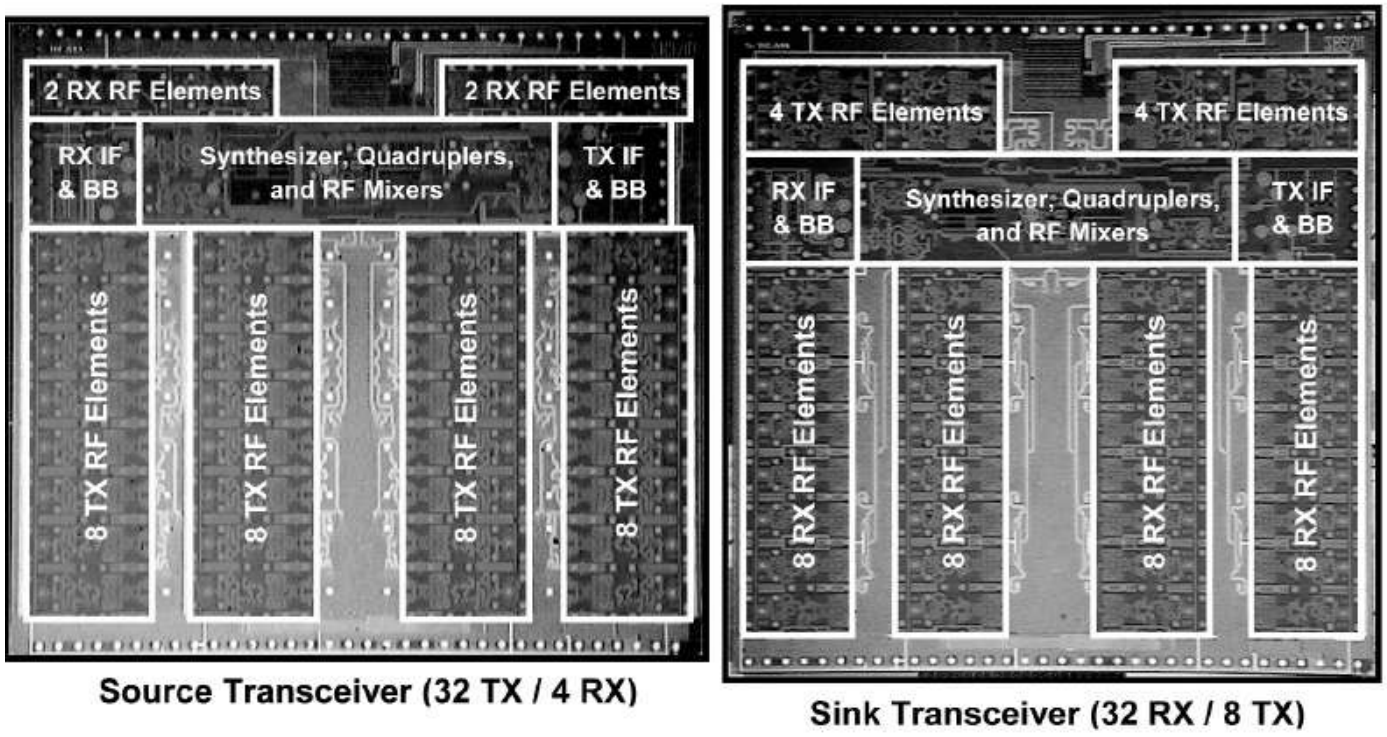
Phase-Array mm-Wave Transceivers

- Phased-Array Architectures
  - RF phase shifting
  - "Pseudo" MIMO (MISO)



Phase-Array mm-Wave Transceivers

- 60 GHz Uncompressed Wireless HD Video Area Network
  - Commercial development (SiBeam)



Source Transceiver (32 TX / 4 RX)

Sink Transceiver (32 RX / 8 TX)

[Enami et al. IEEE ISSCC 2011]

Phase-Array mm-Wave Transceivers

- Evolution timeline

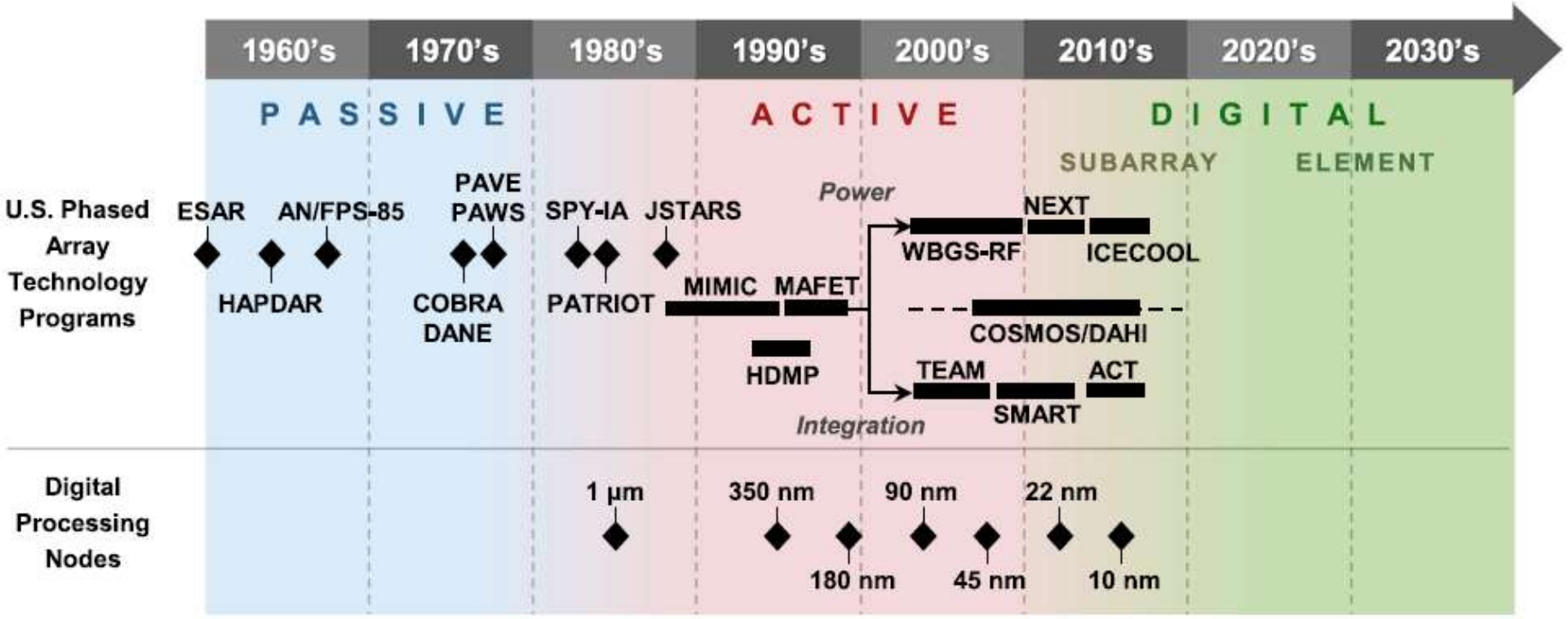


Fig. 1. *U.S. phased array technology development programs and digital processing nodes timeline.*

[Herd et al. Proc. of the IEEE 2016]

Phase-Array mm-Wave Transceivers

- Cost distribution
  - Phased-array: 50%

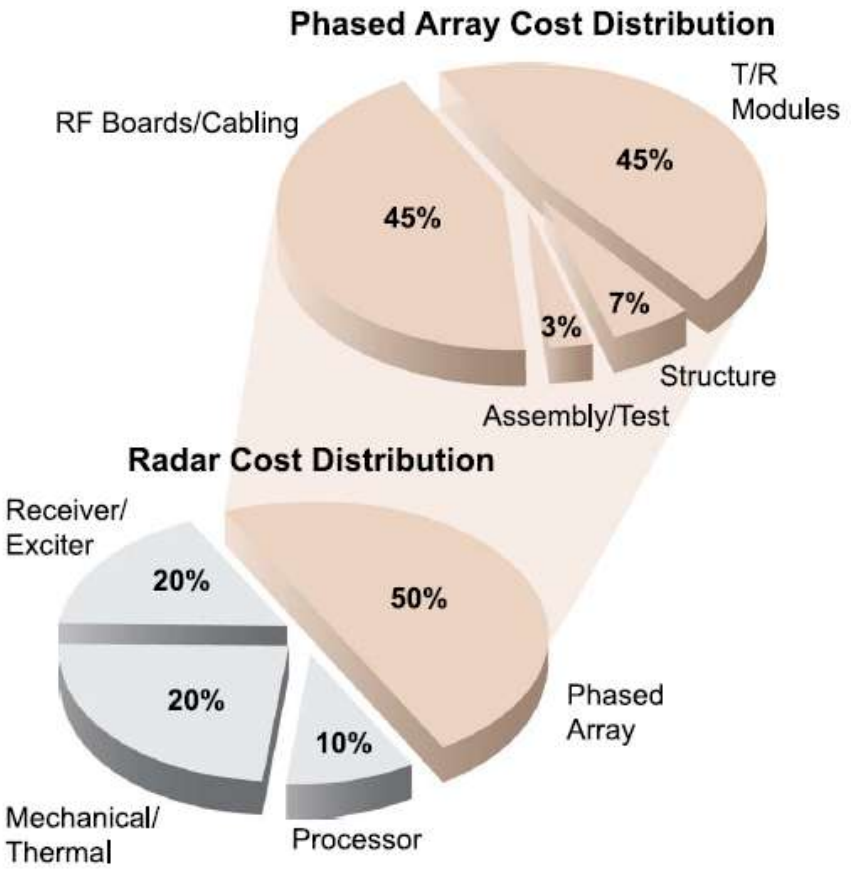
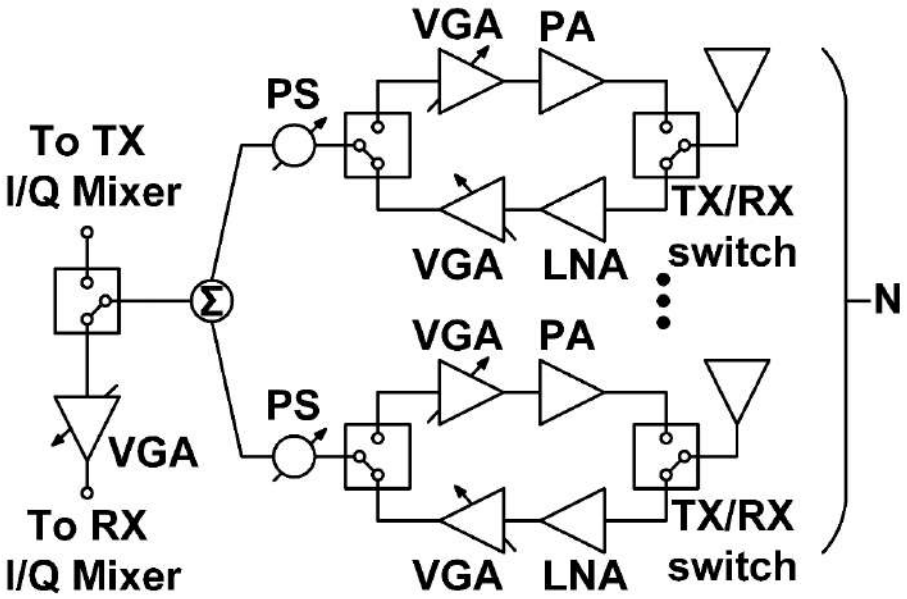


Fig. 9. ***Typical cost distribution for phased array radar.***

[Herd at al. Proc. of the IEEE 2016]

5G/6G Phased-Array Transceivers ICs

- 5G New Radio (NR) standard
  - Freq. Range 2 (FR2): 24.25-52.6 GHz
  - Fosters research on phased-array ICs
- First-reported 28GHz IC for 5G
  - 32 TX/RX (TRX) elements
  - LNA with 12dB gain & 6dB NF (incl. TRX switch losses)
  - Phase-invariant VGA ⇒ beam shaping

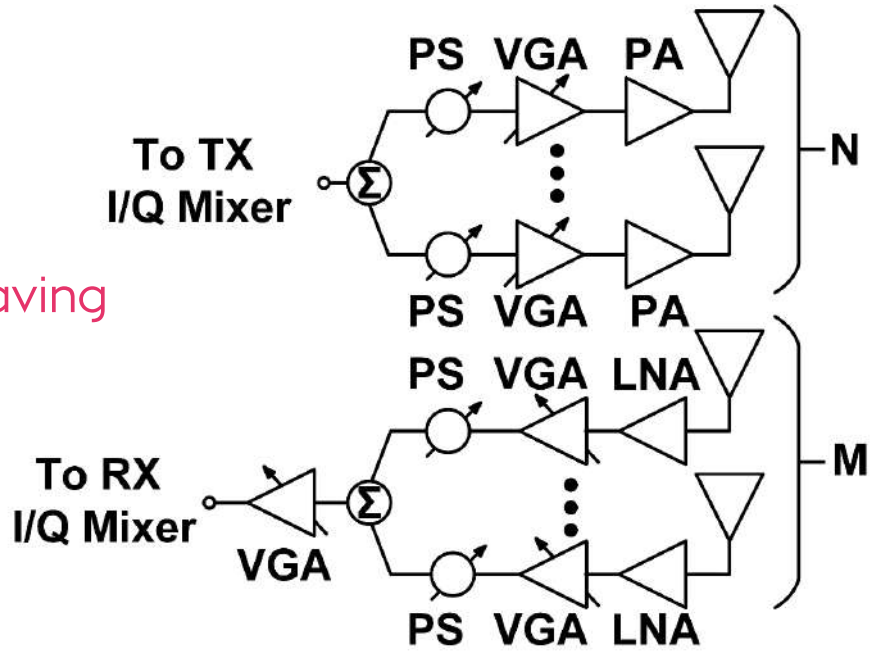


[Sadhu, *IEEE JSSC*, 2017]

[Spasaro and Zito. IEEE IMS 2022]

VG-LNAs for Phased-Array ICs

- ICs with RF phase shifting
  - VG-LNA ⇒ no VGA ⇒ power/area saving
  - Switchless TRX architectures relax gain & NF requirements for LNAs ⇒ Enable low-power designs



- ICs with digital beamforming
  [Gao, IEEE T-MTT, 2021]

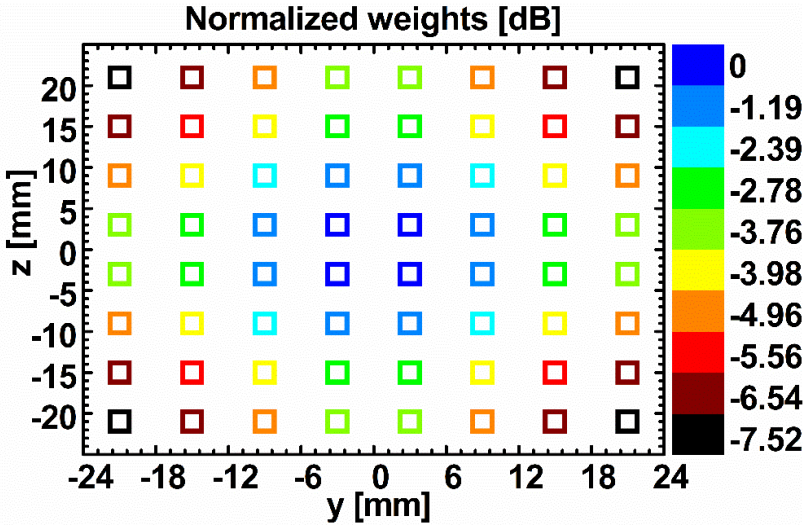
- Compact low-power VG-LNAs are key for 5G/6G RXs
  - Complexity reduction, performance enhancement and functionality extension
  - Cost-effective (small form factor) and energy-efficient (low power) solutions

Sub-mW 30 GHz VG-LNA

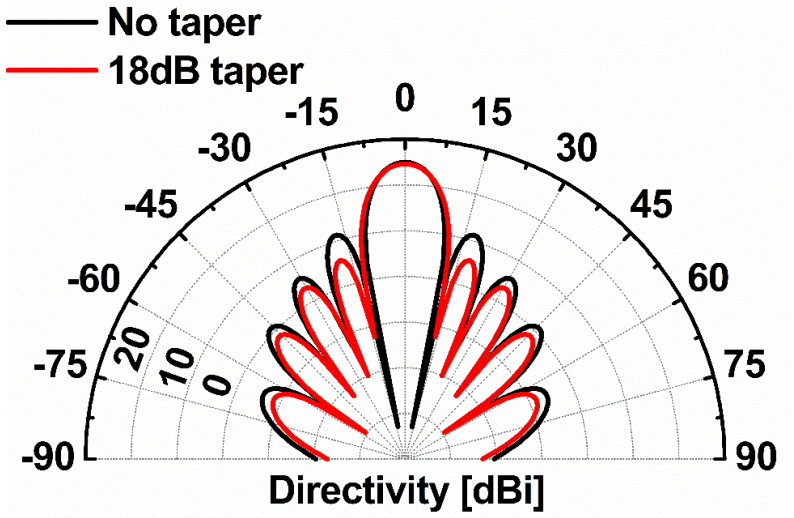
- Prior-art VG-LNAs operating in 5G NR FR2
  - Power consumption: a few/tens of milliwatts
  - Silicon area larger than 0.1 mm^2
- Sub-mW 30GHz VG-LNA in 22nm FDSOI CMOS
  - Core area: 0.044 mm^2
  - Designed for low-power tapered phased array
    - Taylor window taper up to 18 dB
    - Planar 8x8 antenna array

[Spasaro and Zito. IEEE IMS 2022]

Requirements for Gain Control: Tapering



Normalized weights



Radiation pattern of antenna array

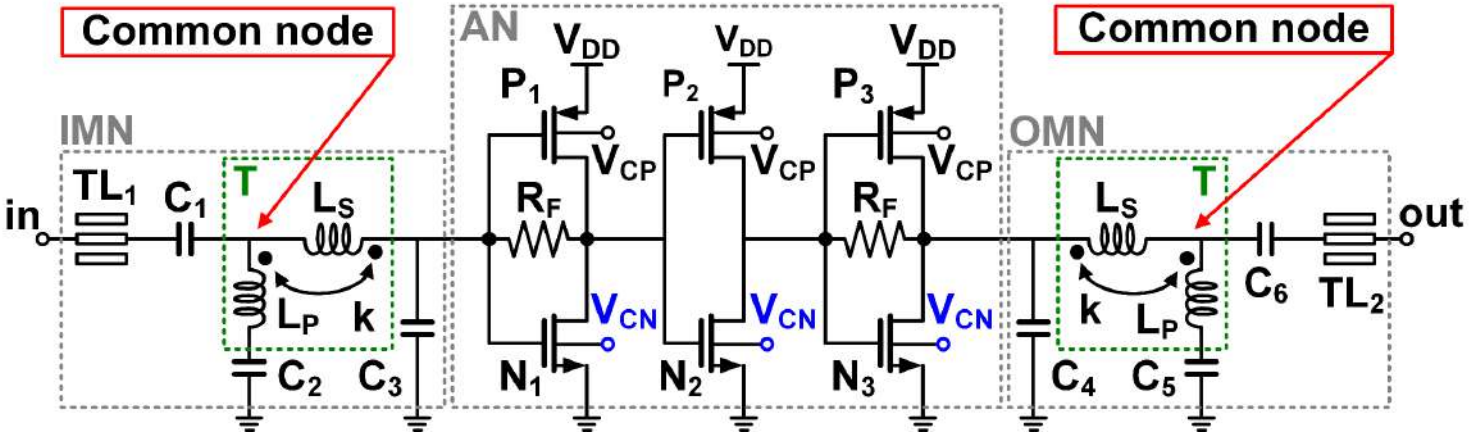
- 30GHz 8×8 3GPP TR 38.901 compliant-antenna array (6mm pitch)
- 18dB Taylor window taper ⇒ 7.5dB gain-control range required

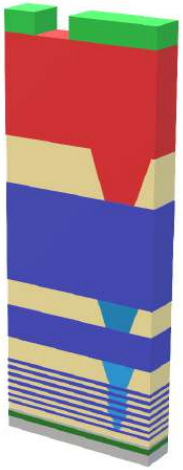
Requirements for Gain Control: VG-LNA

- VG-LNA design goals
  - 8dB gain control range
  - sub-mW P_C for all gain states
  - Peak gain of 16 dB for high-gain state
  - 6dB NF, similarly to other designs [Sadhu, *IEEE JSSC*, 2017]

- In absence of blockers, max. sensitivity condition: Uniform weigths & high gain ⇒ SNR after beamforming network improves by $10\times\text{Log}_{10}(64) = 18$ dB

VG-LNA Features: Circuit





- Inductorless active network (AN)
- Feedworward input (IMN) & output (OMN) matching networks
- Nominal gain of 12 dB with P_C of 0.6 mW
- Single gain-control voltage $V_{CN} = V_C$ (with $V_{CP} = 0$ V)

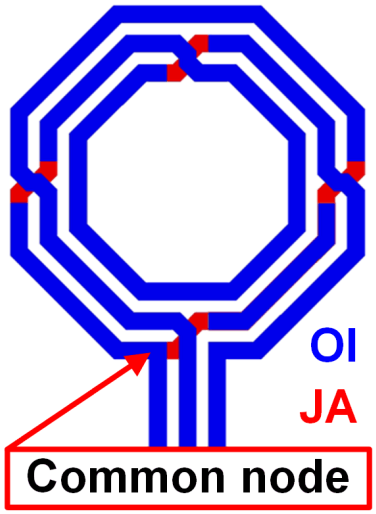
VG-LNA Features: Low-Power Techniques

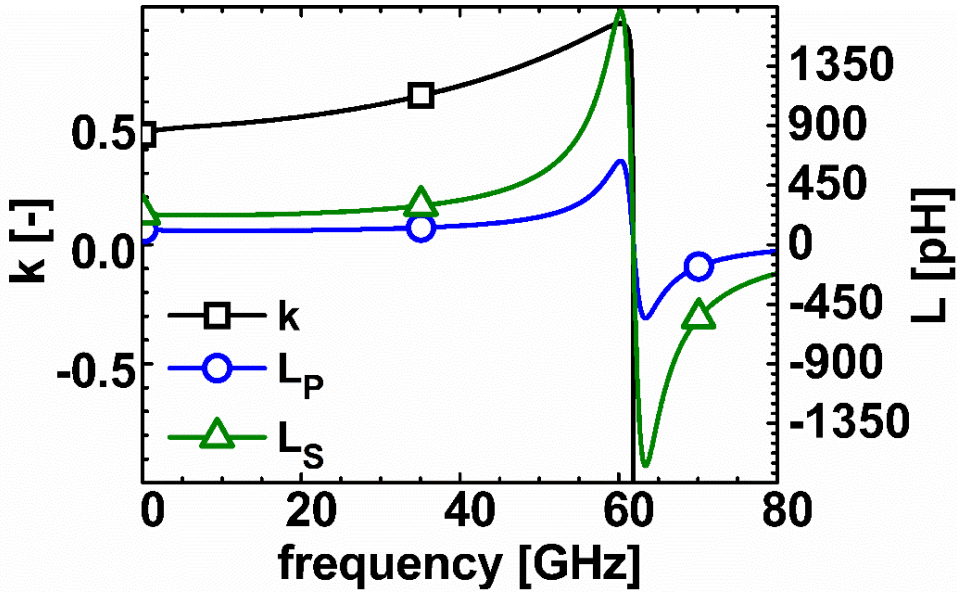
- Inductorless AN with current reuse and three gain stages
  - No peaking inductors or inter-stage matching networks (MNs)
    - Compact layout
    - Reduced parasitics/lossy interconnects

- MNs with cascaded L-network stages and coupled inductors
  - Compact layout
  - Coupling factor (k) & intermediate impedance as free parameters
    - Enable integration and NF optimization

[Spasaro et al. IEEE IMS 2022]
[Spasaro et al. IEEE TCAS-II 2023]

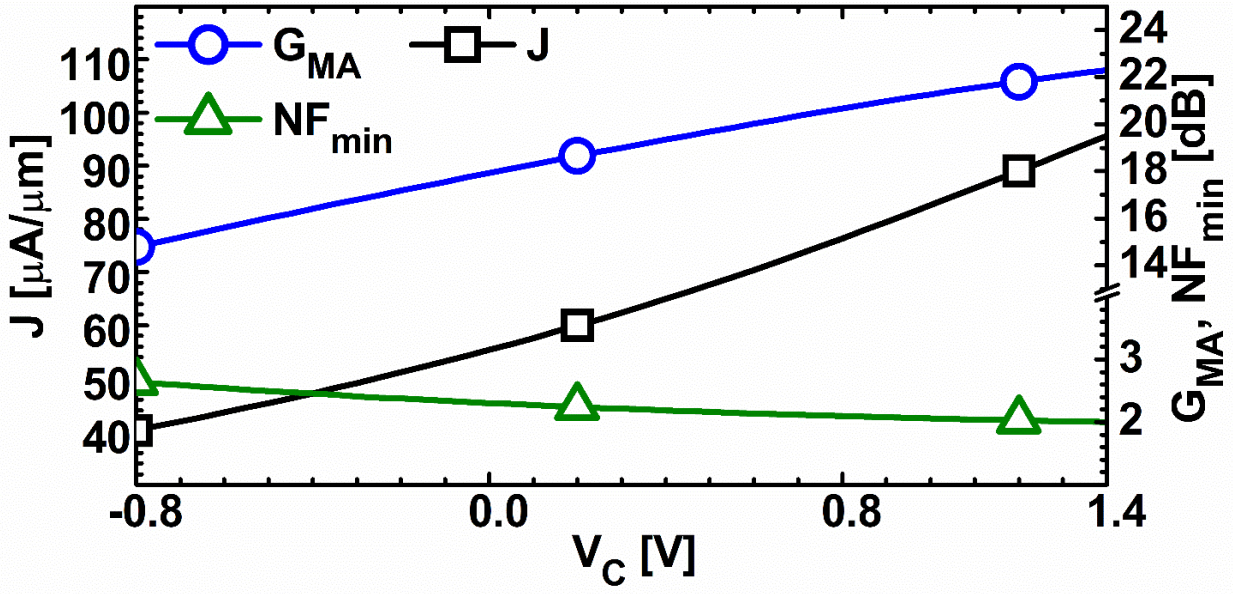
VG-LNA Features: Transformer





- Top-most copper metal layers (JA and OI)
- L_P = 119 pH, L_S = 267 pH, and k = 0.59 at 30 GHz

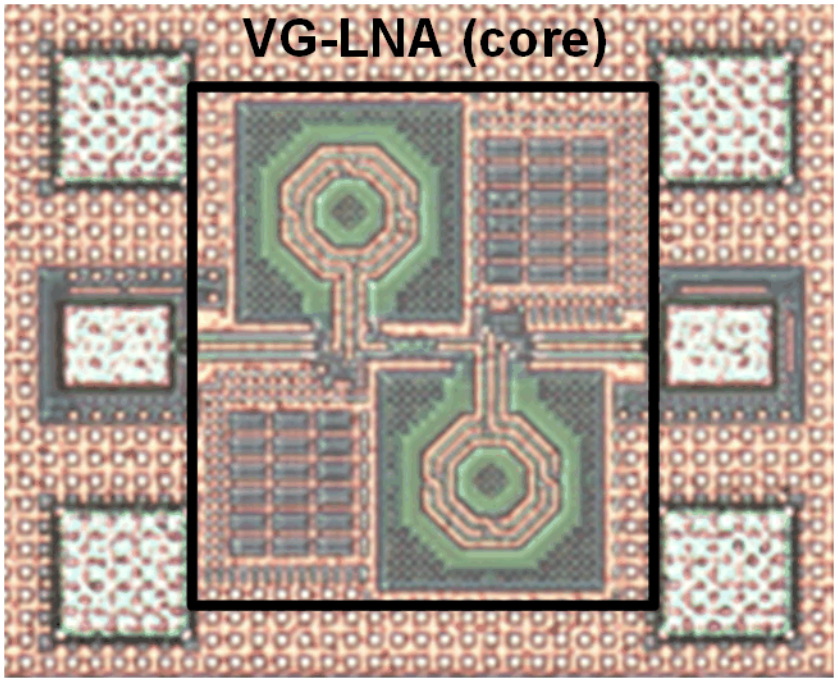
VG-LNA Features: Gain Control



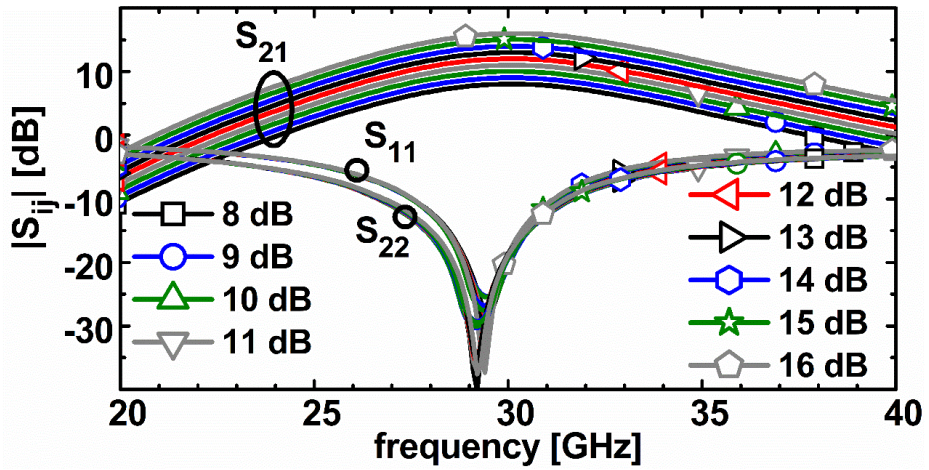
- Post-layout simulations (PLS)
  - Transistor current density (J)
  - Max. available gain (G_{MA}) and NF_{min} of AN at 30 GHz
  - G_{MA} increases from 15 dB to 22 dB as control voltage (V_C) increases

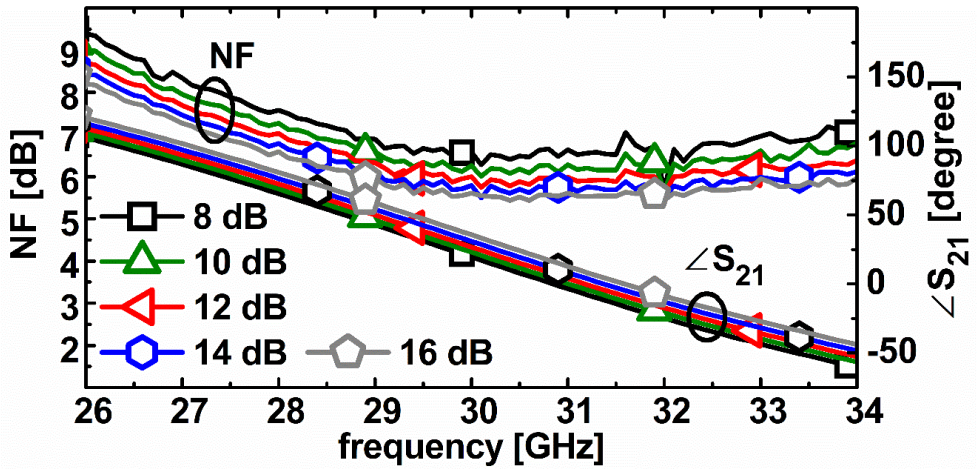
VG-LNA Meas. Results: Test Chip

- Silicon area
  - Core: 0.20×0.22 mm^2
  - With pads: 0.32×0.26 mm^2
- On-die measurements
  - PNA-X N5245A
  - Power meter N1914A
  - Power sensor N8487A
  - ECal N4693A



VG-LNA Meas. Results: S-Parameters & NF



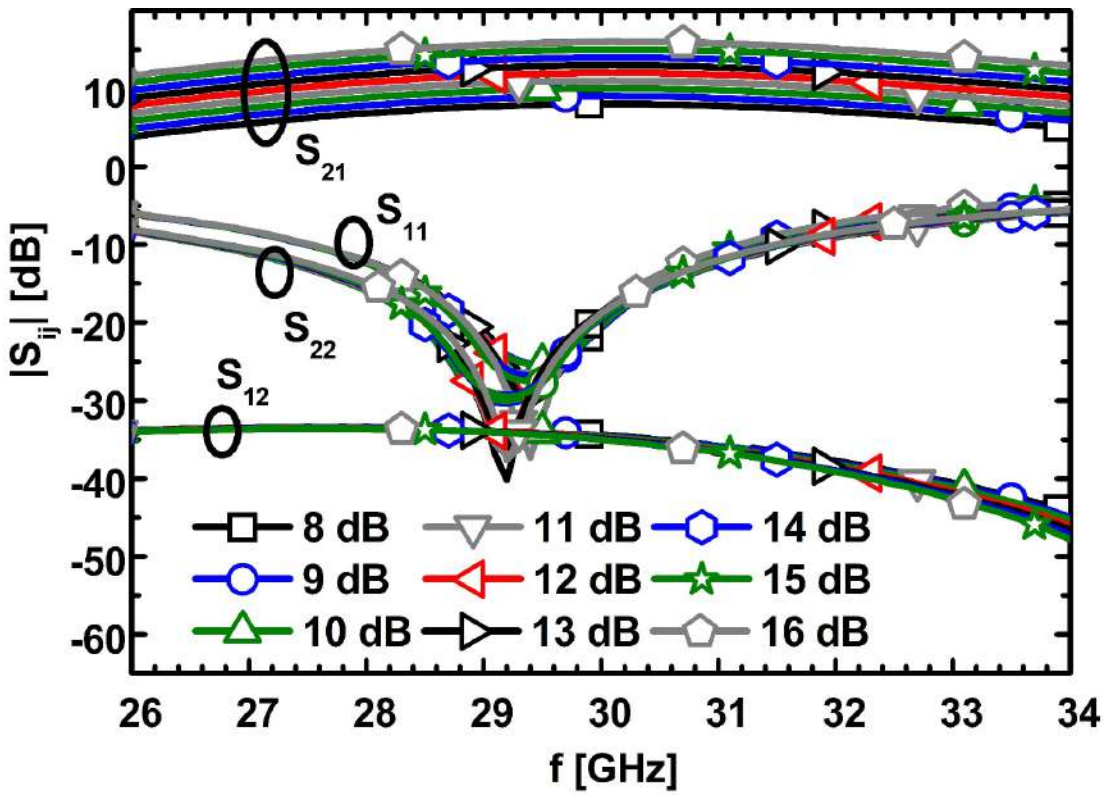


S-parameters

$\angle S_{21}$ and NF

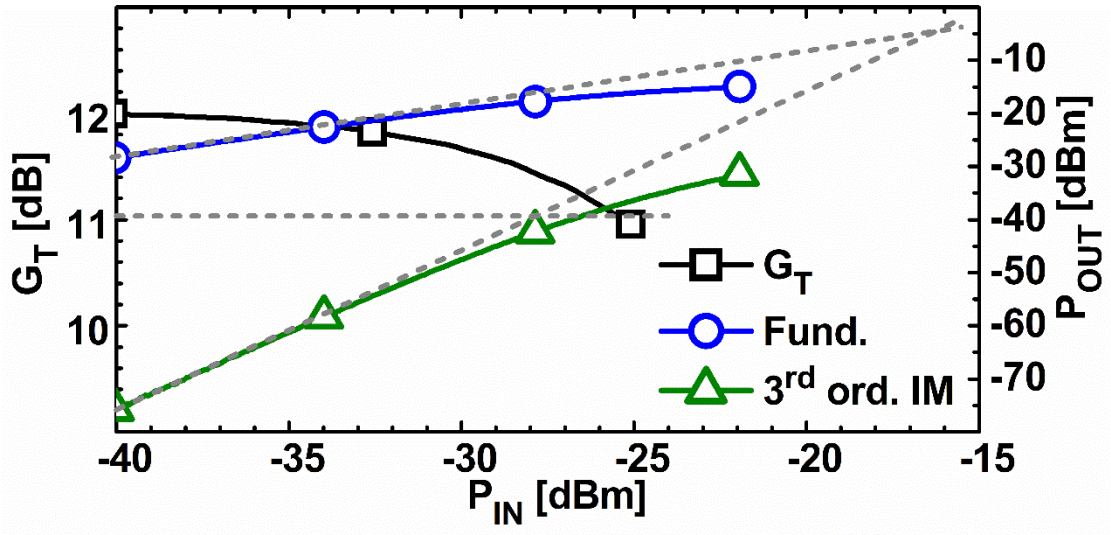
- High gain: S_{21} = 16 dB at 30.1 GHz, NF = 5.5 dB, P_C = 0.97 mW
- Low gain: S_{21} = 8 dB at 30.1 GHz, NF = 6.3 dB, P_C = 0.41 mW
- Variation of $\angle S_{21}$ in the 7GHz BW_{3dB}: $\Delta\varphi_{21} < 16.7°$

VG-LNA Meas. S-Parameters



- Isolation > 30 dB (important result)

VG-LNA Meas. Results: Linearity



Gain [dB]	IP_{1dB} [dBm]	IIP_3 [dBm]
16	-28.8	-19
12	-25.5	-16
8	-21.0	-12

Nominal (12dB gain)

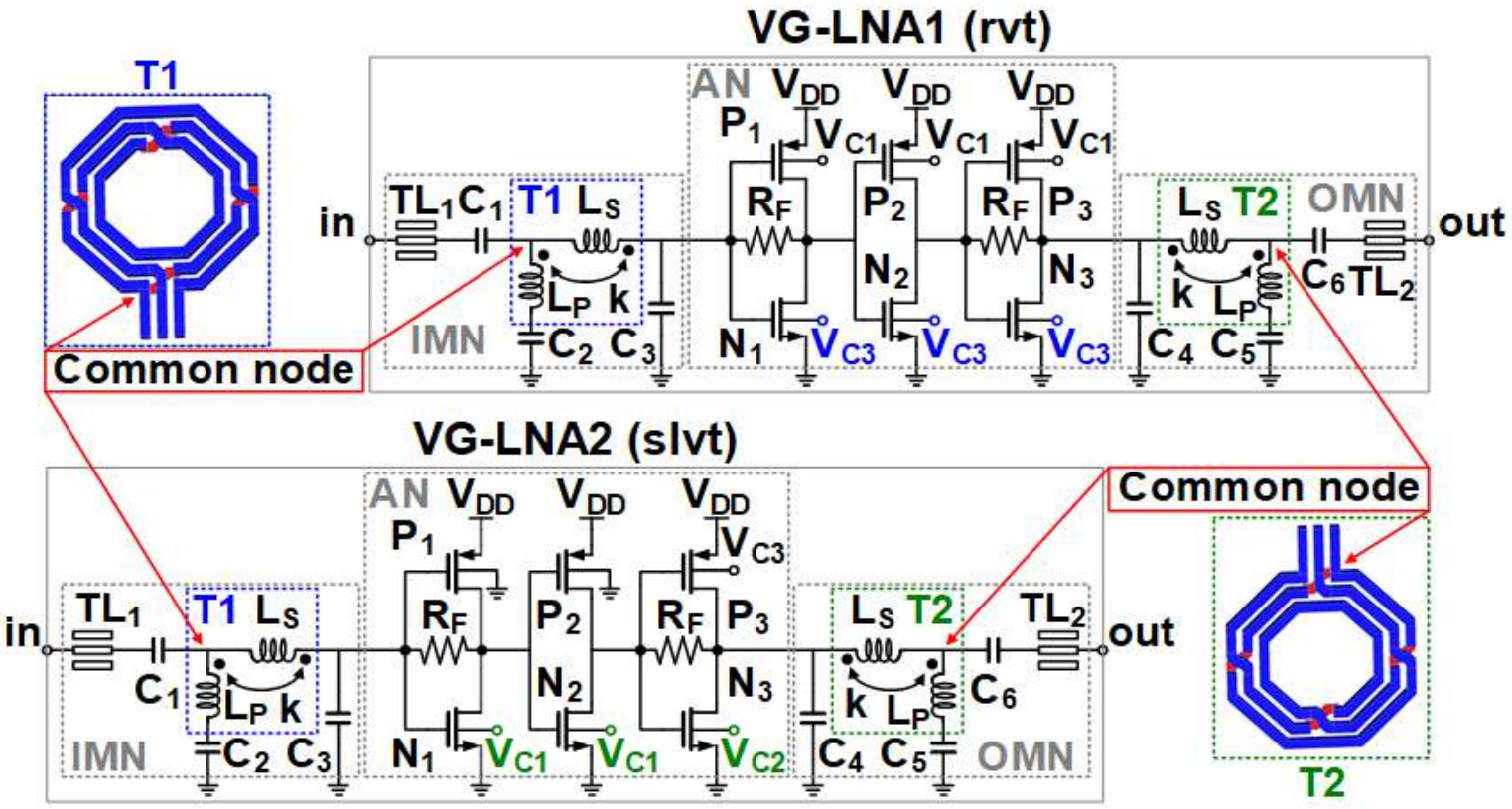
- Transducer gain (G_T) at 30 GHz
- IP_3 for input tones at 30 and 30.05 GHz (as per 5G channelization)

VG-LNA Meas. Results: Comparison with Prior Art

Ref.	Tech. [nm]	S_{21} [dB]	f_C [GHz]	BW_{3dB} [GHz]	NF [dB]	IP_{1dB} [dBm]	$\Delta\varphi_{21}$ [°]	P_C [mW]	Area [mm²]
This	22 FDSOI	16 8	30.1 30.1	7.1 7.2	>5.5 >6.3	-28.8 -21.0	16.7	0.97 0.41	0.044
[T-MTT, 2021][1]	22 FDSOI	24.2 16.2	30.4 30.4	23.7 23.7	>2.4 >3.0	-25 -19	-	16 16	-
[MWCL, 2018]	40 Bulk	27.1 18.4	27.1 27.8	7.4 9.3	>3.3 >3.4	-21.6 -13.4	18	31.4 21.5	0.26
[MWCL, 2019]	65 Bulk	20.8 10.2	30.4 30.4	4 4	>3.7 -	-20.4 -	8	26.7 16.5	0.20
[IMS, 2021]	90 Bulk	21.4 11.6	37 37	11.3 11.3	>4.7 -	-25.1 -22	7.2	17.9 17.9	0.45[2]
[IWS, 2021]	65 Bulk	11.4 -5	28 28	11.5 -	>4.7 -	-	-	2.16 -	0.13

[1]Simulation results; [2]including pads

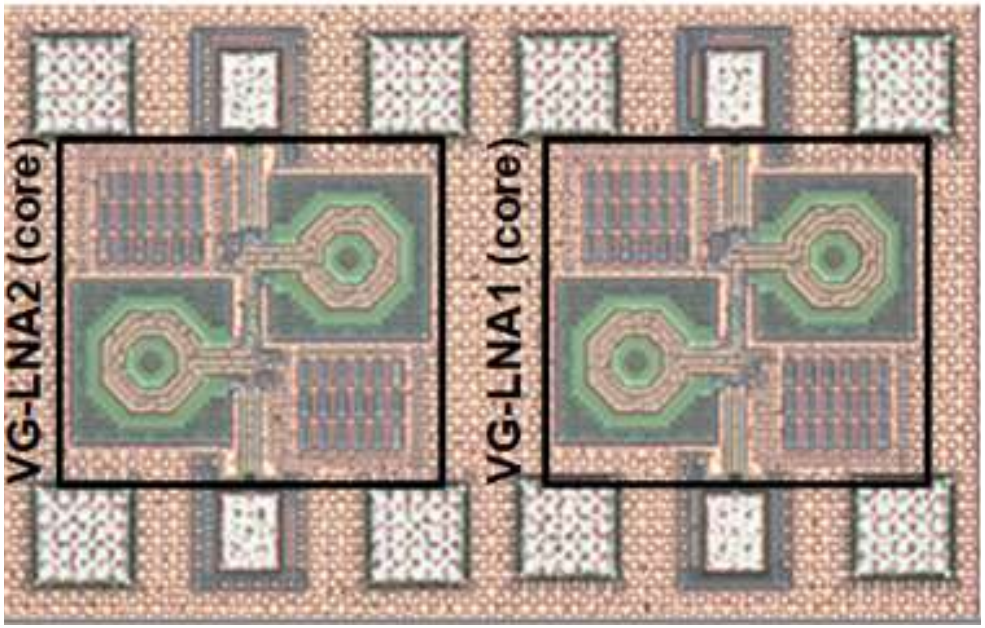
Benchmarking and Validation: rvt vs. slvt MOSFETs



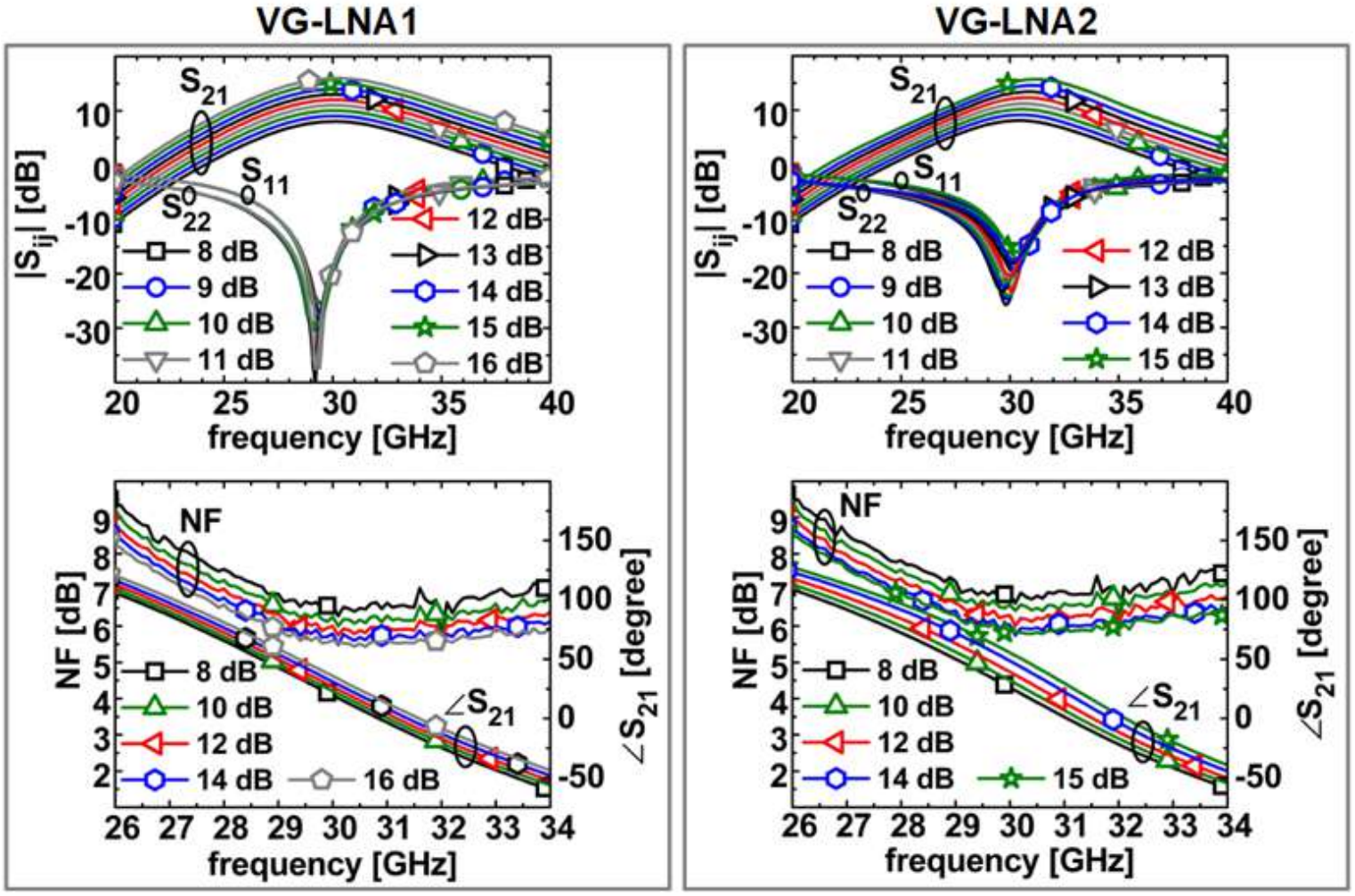
- Inductorless active network (AN), with IMN & OMN
- 12dB nominal gain with P_C = 0.6 mW
- Single gain-control voltage: VG-LNA1 (V_{C1}=0 V, V_{C3}=V_C); VG-LNA2 (V_{C3}=0 V, V_{C1}=V_{C2}=V_C)

[Zito et al. IEEE DTTIS 2024]

Benchmarking and Validation: Test Chips

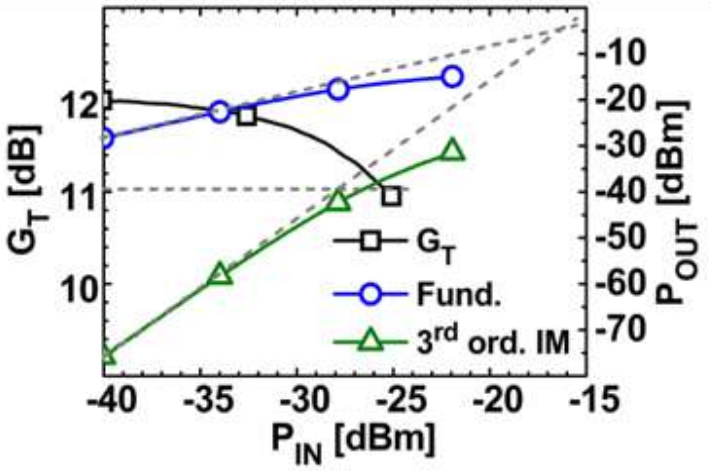


Benchmarking and Validation: Perfomance (1/2)



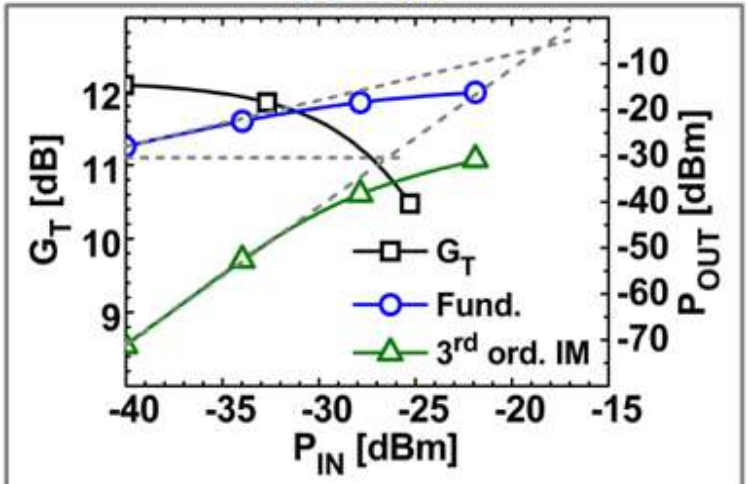
Benchmarking and Validation: Performances (2/2)

VG-LNA1



V_C [mV]	Gain [dB] @30GHz	IP_{1dB} [dBm]	IIP_3 [dBm] @50MHz	IIP_3 [dBm] @100MHz	IIP_3 [dBm] @200MHz	IIP_3 [dBm] @400MHz
-740	8.0	-21.0	-12	-11	-9	-6
-530	9.0	-22.3	-13	-12	-10	-8
-310	10.0	-23.5	-14	-13	-12	-11
-92	11.0	-24.5	-15	-14	-13	-13
152	12.0	-25.5	-16	-15	-15	-14
403	13.0	-26.3	-17	-16	-16	-16
683	14.0	-27.2	-18	-17	-17	-17
1003	15.0	-28.0	-19	-18	-18	-18
1340	16.0	-28.8	-19	-19	-19	-19

VG-LNA2



V_C [mV]	Gain [dB] @30GHz	IP_{1dB} [dBm]	IIP_3 [dBm] @50MHz	IIP_3 [dBm] @100MHz	IIP_3 [dBm] @200MHz	IIP_3 [dBm] @400MHz
-255	8.0	-22.7	-13	-13	-12	-12
-92	9.0	-24.1	-15	-14	-14	-14
70	10.0	-25.2	-16	-15	-15	-15
260	11.0	-26.3	-17	-17	-17	-16
479	12.0	-27.4	-18	-18	-18	-18
739	13.0	-28.4	-19	-19	-19	-19
1065	14.0	-29.4	-21	-21	-21	-20
1600	15.0	-30.5	-22	-22	-22	-21

Benchmarhing and Validation: Comparison with Prior-Art VG-LNAs in 5G NR FR2

Work	VG-LNA2		VG-LNA1 [6]		[2][1]		[3]		[4]		[5]		[19]	
CMOS Tech. [nm]	22 (FDSOI)		22 (FDSOI)		22 (FDSOI)		40 (Bulk)		65 (Bulk)		90 (Bulk)		65(Bulk)	
Peak gain [dB]	15.7	8.1	16	8.0	24.2	16.2[2]	27.1	18.4	20.8	10.2	21.4	11.6	11.4	-5
f_c [GHz]	31.2	30.4	30.1	30.1	30.4[5]	30.4[5]	27.1	27.8	30.4[2]	30.4[2]	37	37[2]	28	28
BW_{3dB} [GHz]	5.7	6.4	7.1	7.2	23.7	23.7[2]	7.4	9.3	4	4[2]	11.3[4]	11.3[2]	11.5	-
Min. NF [dB]	5.9	6.9	5.5	6.3	2.4	3.0	3.3	3.4	3.7	-	> 4.7	-	> 4.7	-
IP_{1dB} [dBm]	-30.5[3]	-22.7[3]	-28.8[3]	-21.0[3]	-25	-19	-21.6	-13.4	-20.4	-	-25.1[5]	-22[2]	-	-
$\angle S_{21}$ variation* [°]	29.5		16.7		-		18		8		7.2		-	
P_C [mW]	0.91	0.40	0.97	0.41	16	16	31.4	21.5	26.7	16.5	17.9	17.9	2.16	-
Core area [mm^2]	0.044		0.044		-		0.26		0.20		0.45[6]		0.13	

[1]Simulation results; [2]deduced from plots; [3]measured at 30 GHz; [4]dual band (26-30.5 GHz and 33.8-40.6 GHz)
[5]calculated from available data; [6]including pads; *max variation in 3dB band.

VG-LNA: Conclusions

- 30GHz VG-LNA with 8dB gain-control range
  - Record power consumption (world-1st sub-mW) and area on silicon
  - Compliant with targeted tapered phased-array IC with switchless TRXs
  - 4-to-32 VG-LNA units consume less than one unit of prior-art VG-LNAs
  - Very compact size (one or more orders of magnitude)
  - S_{21} phase variation, IP_{1dB}, BW_{3dB}, & NF comparable with prior works
  - Benchmarging and validation across technology flavours (rvt and slvt)
  - Higher frequency limitations

Conclusions

- Ultra-scaled Silicon techs show the largest potentional as platform for many current and future emerging technologies (e.g. wireless and quantum), but the losses require innovative topologies and loss-aware design methodologies

- Our ultimate innovative (new design paradigm) building blocks with world-record performance – These have open new technology developments and technology directions (Wireless, IoTs & Quantum) – transistor-size low-power mm-wave ICs

Acknowledgments

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