50 Shades of Delta Sigma

Chadi Jabbour

ICE 2026
7th of May 2026

Outline

What are Delta Sigma Modulators ?

From Analog to Digital

High speed Delta Sigma DACs

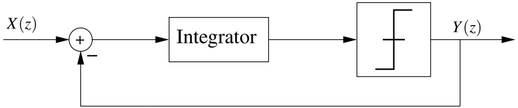
Spatio-temporal DSM in a massive MIMO system

Conclusion

What is Delta Sigma ?

Simple ! !

It is a Delta so a subtraction and a Sigma so addition and that is that



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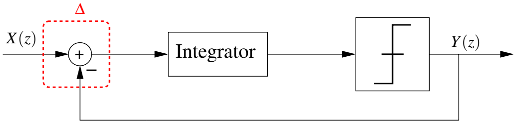

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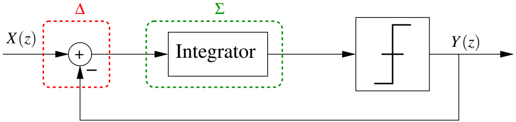

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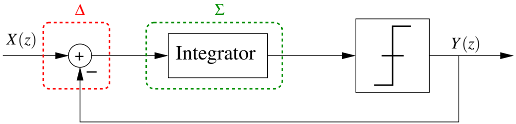
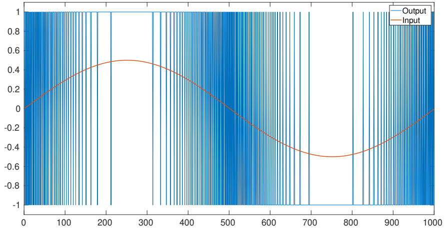
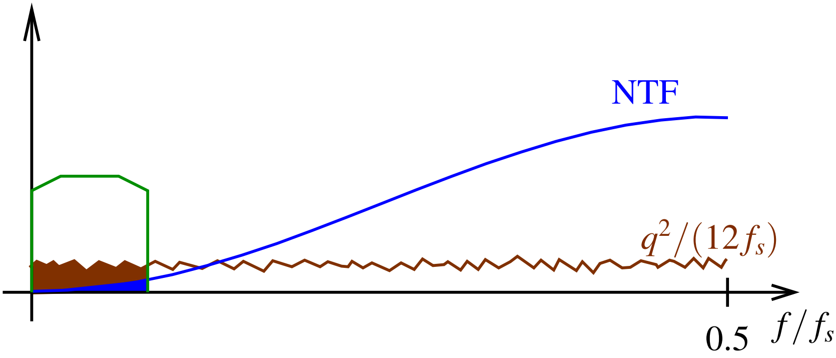




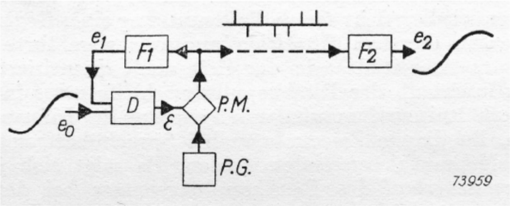
Noise Shaping



Delta Sigma modulation is based on oversampling and noise shaping

History

- Delta Sigma is somehow the successor of Delta modulation



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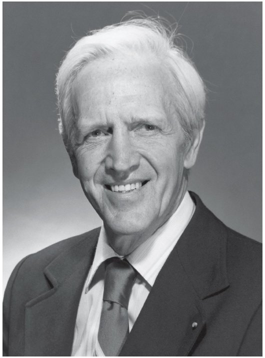

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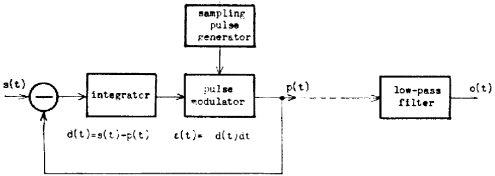
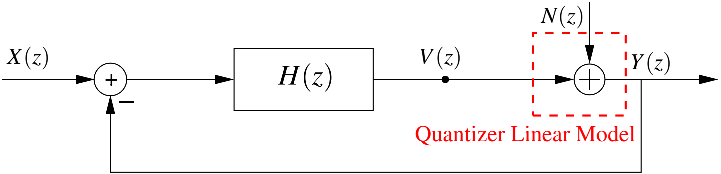
- The architecture was named Delta Sigma in 1961 by Inose and Yasuda



Noise and Signal Transfer function : NTF/STF



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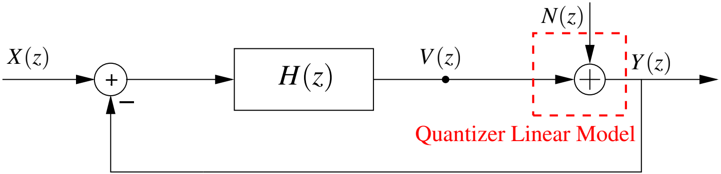

$$Y(z) = \underbrace{\frac{H(z)}{1+H(z)}}_{STF(x)} X(z) + \underbrace{\frac{1}{1+H(z)}}_{NTF(x)} N(z)$$

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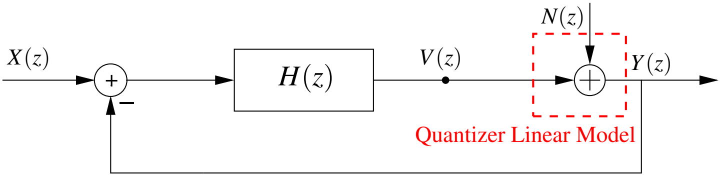

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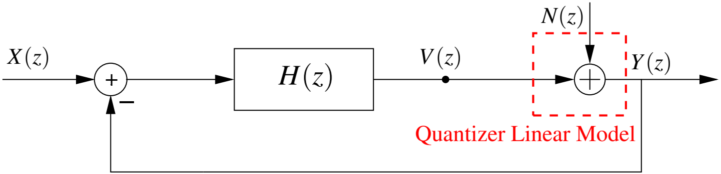

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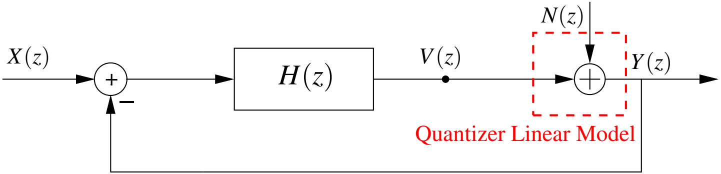

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$$\mid STF(f) \mid = 1 \quad \mid NTF(f) \mid = \mid 2\sin(\pi f T_s) \mid$$

Delta Sigma : degrees of freedom

Assuming $NTF(z) = (1 - z^{-1})^{order}$

$$SNR = 20\log\left(\frac{AmpIn}{FS}\right) + 3.02(2 \cdot order + 1)log2(OSR) + 6.02 \cdot nbits$$
$$+1.76 + 10\log(2 \cdot order + 1) - 9.94 \cdot order$$

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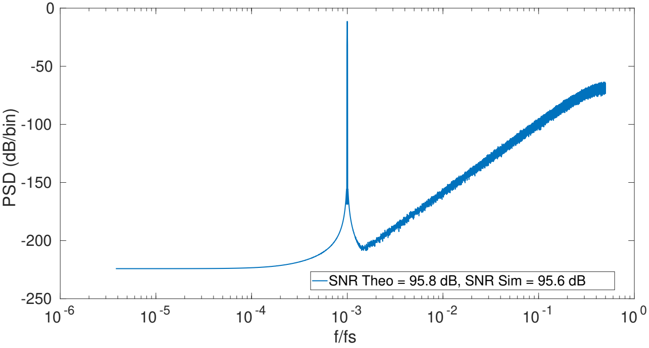

Order=3 ; Amp=-6 dBFS ; nq = 5 bits

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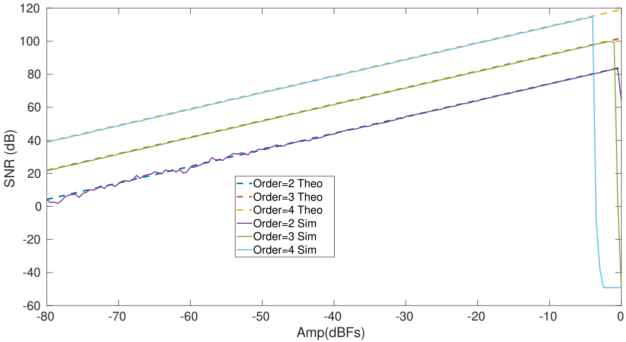

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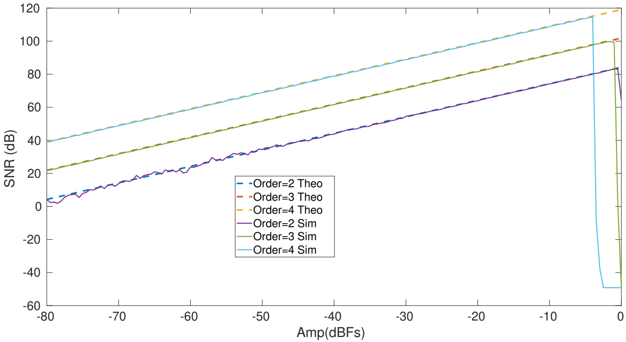

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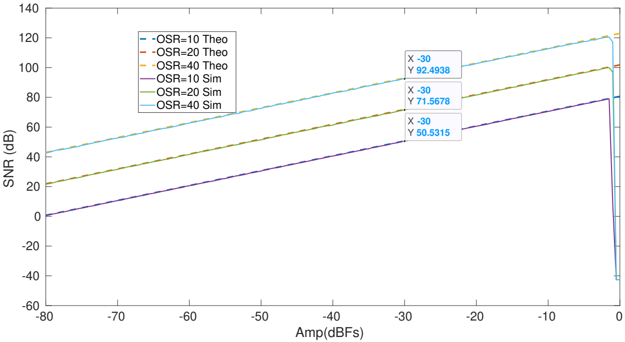

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Delta Sigma : zero optimization

$$SNR = 20\log\left(\frac{AmpIn}{FullScale}\right) + 3.02(2\cdot order+1)log2(OSR) + 6.02\cdot nbits$$
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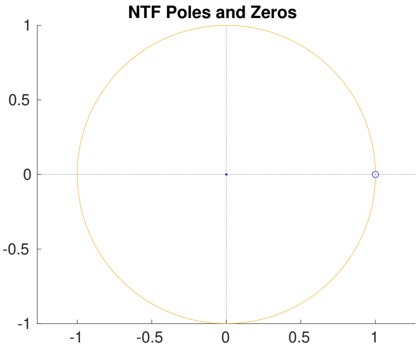

Order=3 ; OSR=20 ; no zero optimization

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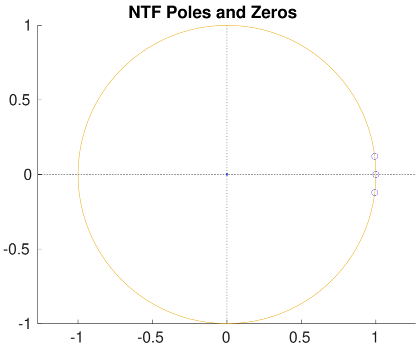

Order=3 ; OSR=20 ; with zero optimization

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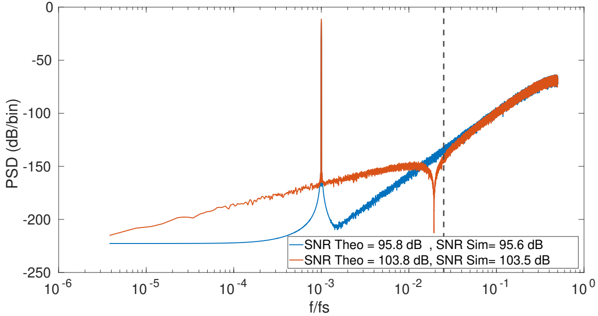
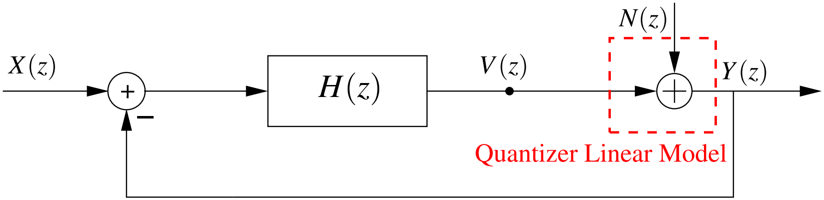


Order3 ; OSR=20 ; nq = 5 bits

Order	1	2	3	4	5
OptExtraSNR (dB)	0	5	8	13	18

Unstability : why ? (with a lot of approximations)



$$V(z) = STF(z) \cdot X(z) + (NTF(z) - 1) \cdot N(z)$$

Assuming a $STF(z) = 1$, $NTF(z) = (1 - z^{-1})^{order}$ and $P_N(z) = \frac{q^2}{12} = \frac{FullScale^2}{2^{2nq}12}$, the higher the order, the lower nq, the higher the probability for $V(z)$ to exceed the quantizer full scale leading to unstablility.

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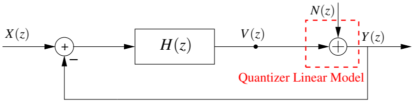

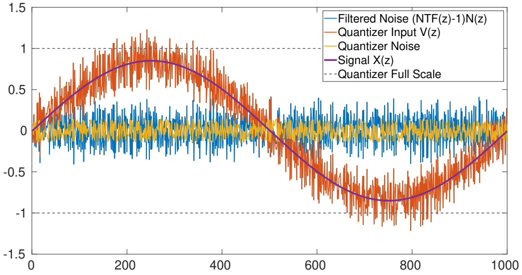

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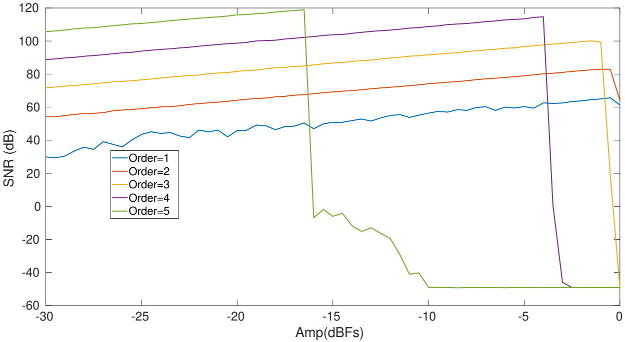
Stability : How ? Nbits/Gain



OSR=20 ; nq = 5 bits ; Hinf=2^{order}

- **Reduce the order $\rightarrow$ lower SQNR**
- Increase the quantizer number of bits $\rightarrow$ higher complexity
- Reduce $NTF(z)$ gain by adjusting the denominator $NTF(z) = \frac{(1-z^{-1})^{order}}{D(z)}$ $\rightarrow$ lower SQNR

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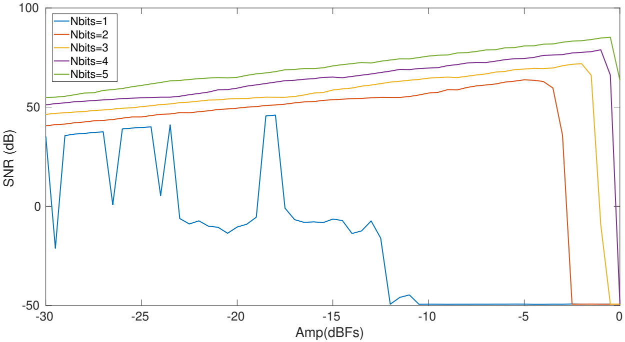

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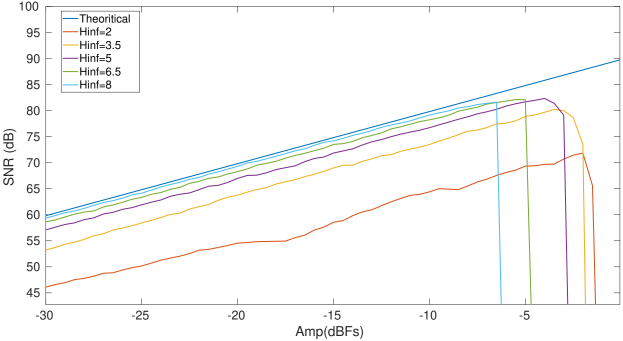

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Stability : theories

Lot of complex theories

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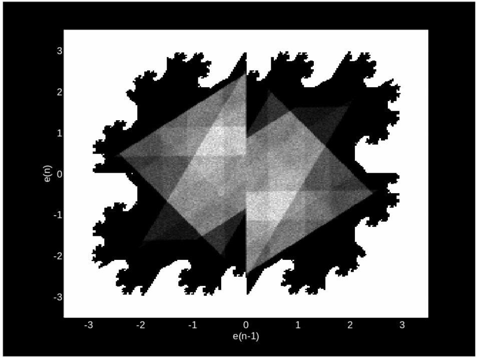
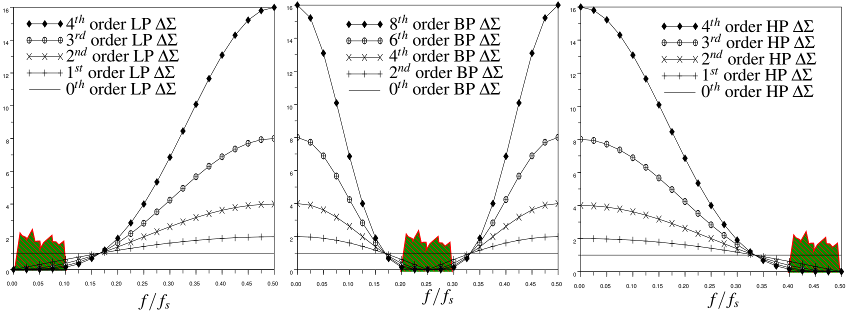


It is better to have beautiful figure that nobody understands

Noise Shaping types



Delta sigma modulation can be changed between low pass, high pass ($f_0 = f_s/2$) or bandpass ($0 < f_0 < f_s/2$) by adjusting the NTF/STF

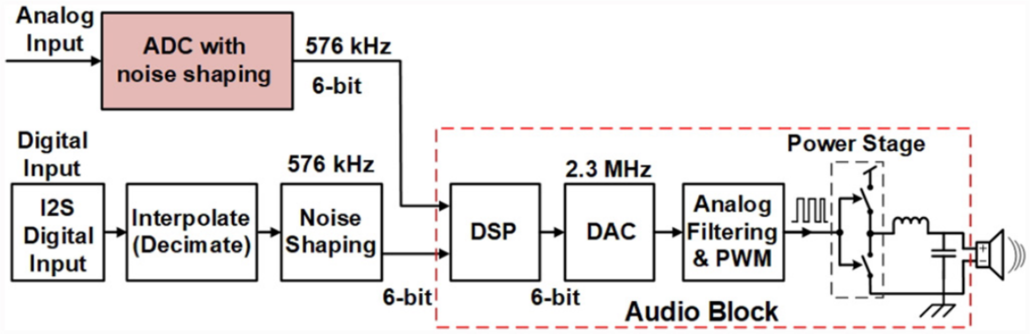
Design methodologies

Many other design or simulation toolbox were proposed :

- F. Medeiro in 1994 : Multi-level design tool
- K. Francken et al in 2003 and 2005 : Top-down/bottom-up First tool
- M. Ortmanns et al in 2015 : Online Sigma-Delta Synthesis Tool
- M.T. Nguyen et al in 2016 : Design methodology for Delta Sigma based Receivers
- D.K.G. Pham et al in 2017 : Open source simulation tool for Continuous Time modulator
- B. Cortes-Delgadillo et al in 2018 : Improved SIMSIDES with genetic algorithms
- J. De La Rosa in 2022 : Design using Machine Learning

Many tradeoffs : suitedness (ADC, DAC, DT, CT, Receivers, ...), speed, accuracy, ease of use, ...

How can it be used ?



An Incremental- ADC With 106-dB DR for Reconfigurable Class-D Audio Amplifiers - Quereshy et al. 21

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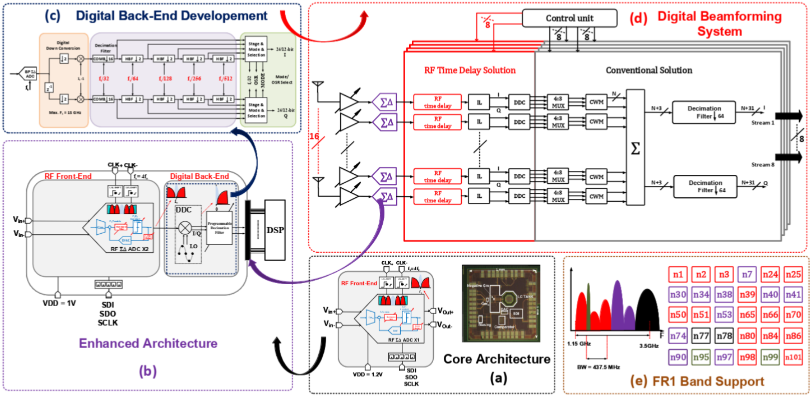

RF to Bits Highly Tunable Sub-1 pJ/bit Digital Beamforming Receiver Architectures for 5G Applications - Ghoniem et al. 22

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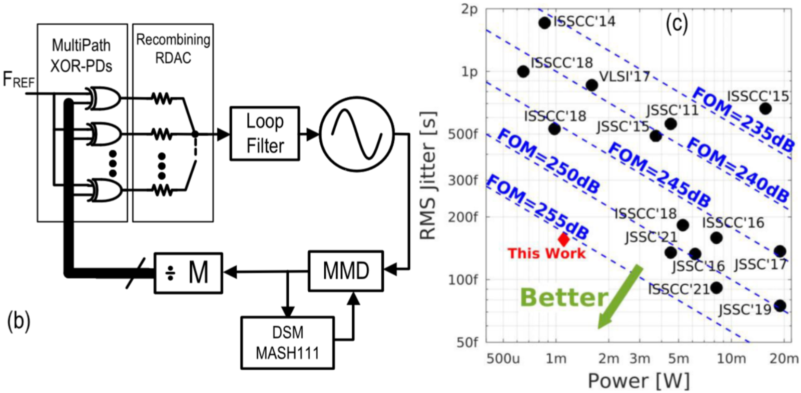

A Calibration-Free Fractional-N Analog PLL With Negligible DSM Quantization Noise - Murphy et al. 23

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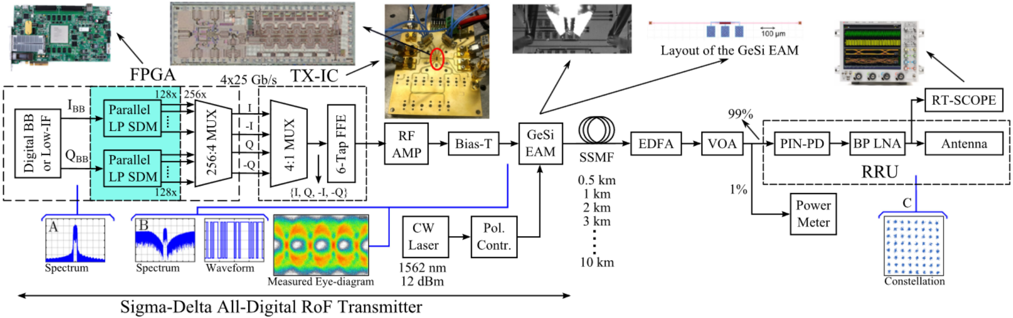

Real-Time 100-GS/s Sigma-Delta Modulator for All-Digital Radio-Over-Fiber Transmission - Li et al. 19

And more ?

- Analog to Digital conveters/Direct Receivers
- Digital to analog Converters/Direct Transmistters
- Digital Pre-Distortion
- Digital Power Conversion
- Closed-loop MEMS actuation
- Neuromorphic applications
- Voltage controlled Oscillators
- and many others

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From Analog to Digital

High speed Delta Sigma DACs

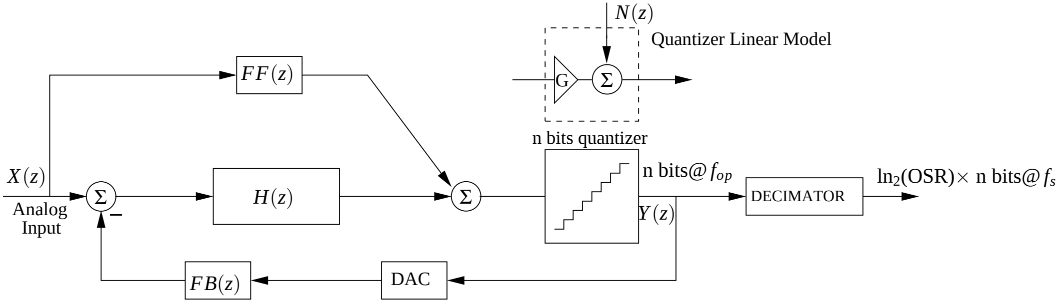
Spatio-temporal DSM in a massive MIMO system

Conclusion

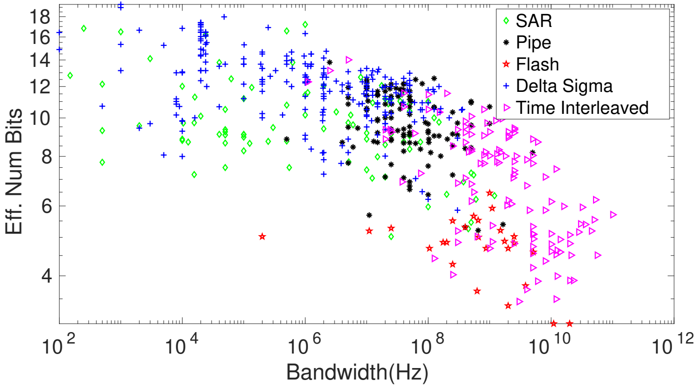
From analog to digital

From Analog to digital

One the main application of delta Sigma Modulators are to convert a signal from analog to digital



ADC performance : VLSI-ISSCC from 1997 to 2024



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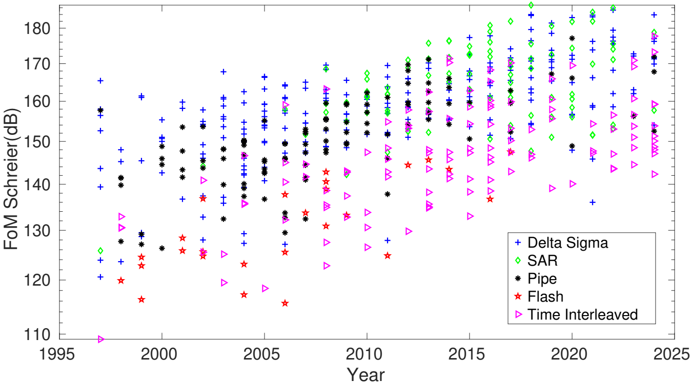

Thermal or Schreier Figure of Merit

$$FOM = SNDR + 10\log\left(\frac{Bw}{P}\right)$$

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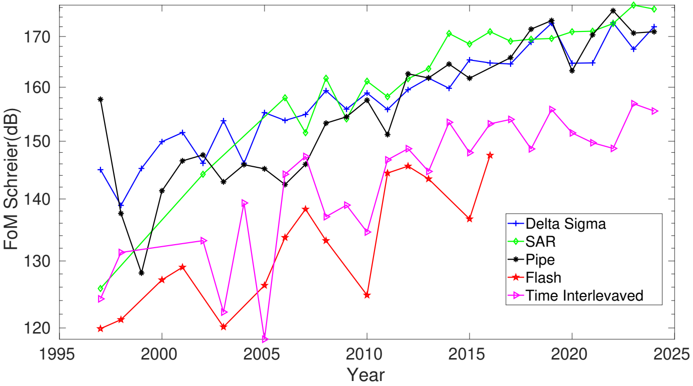

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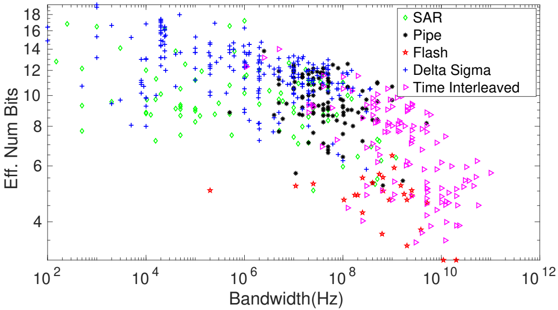
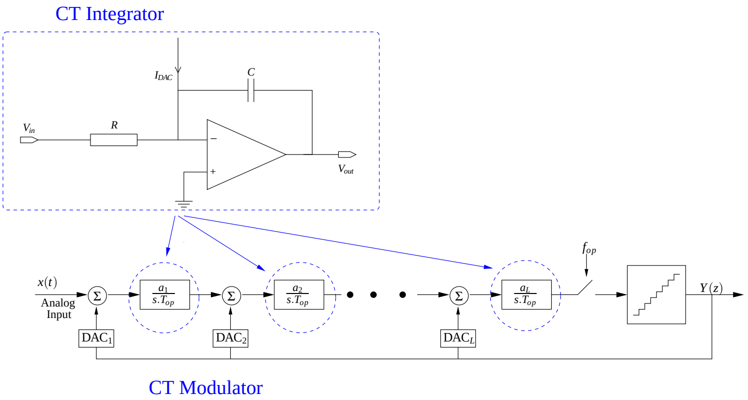


DSM use

DSM are used for high resolution low/average speed ADC with very good power efficiency

DSM ADC are thus excellent candidates for applications Audio, wireless communication, automotive, ...

Discrete Time vs Continuous Time Implementations



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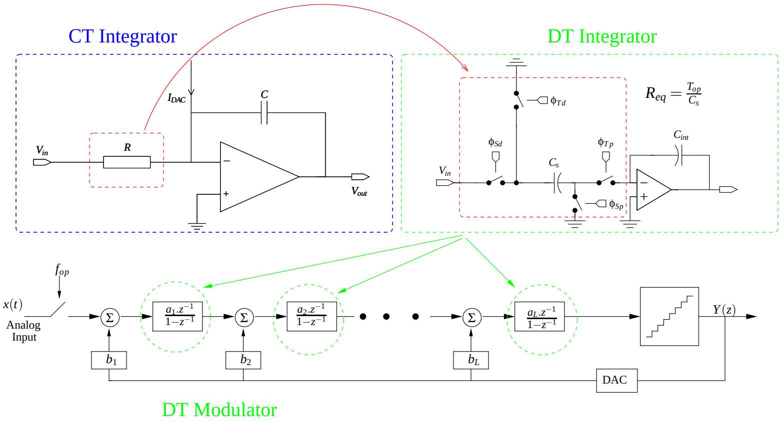

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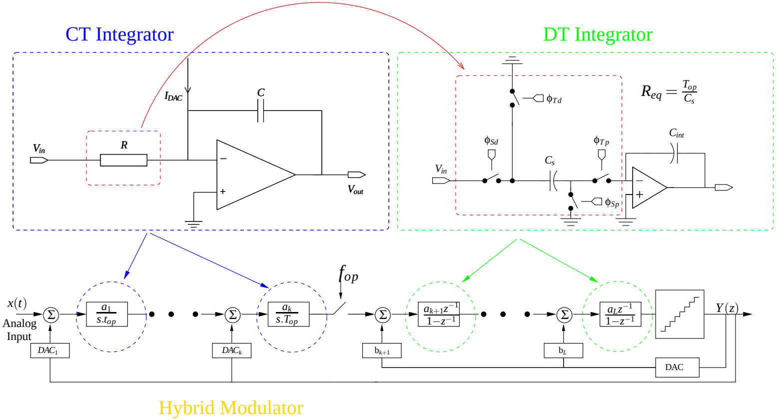
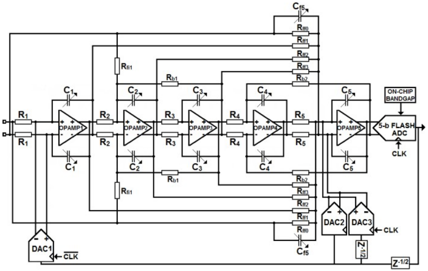
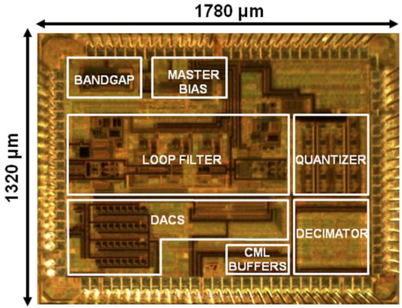


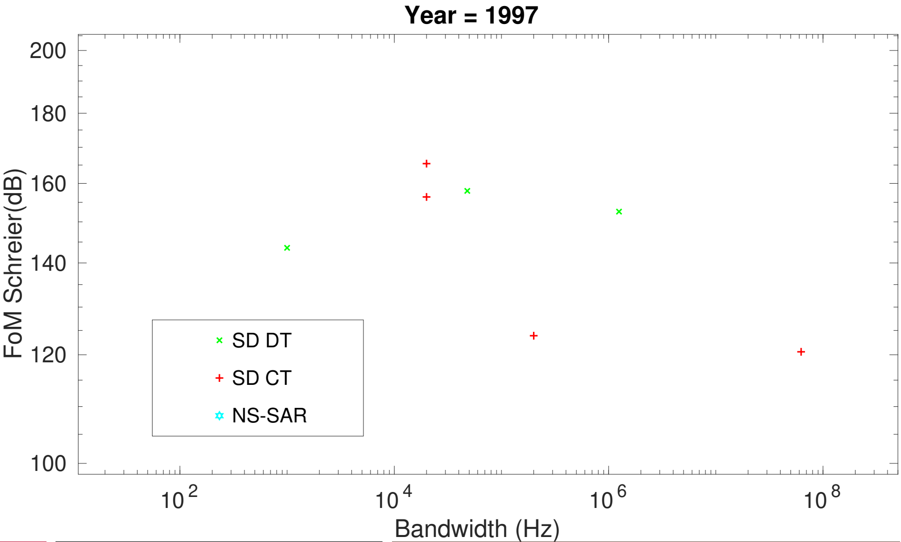
Startup Nation





- A 11-bit 80/40/20 MS/s 5th order OSR-8 ΔΣ ADC implemented in a 65 nm CMOS technology
- IC integrates on chip calibrations, decimator and bandgap
- It was the founding stone to start SCALINX in 2015

Evolution of the SOA



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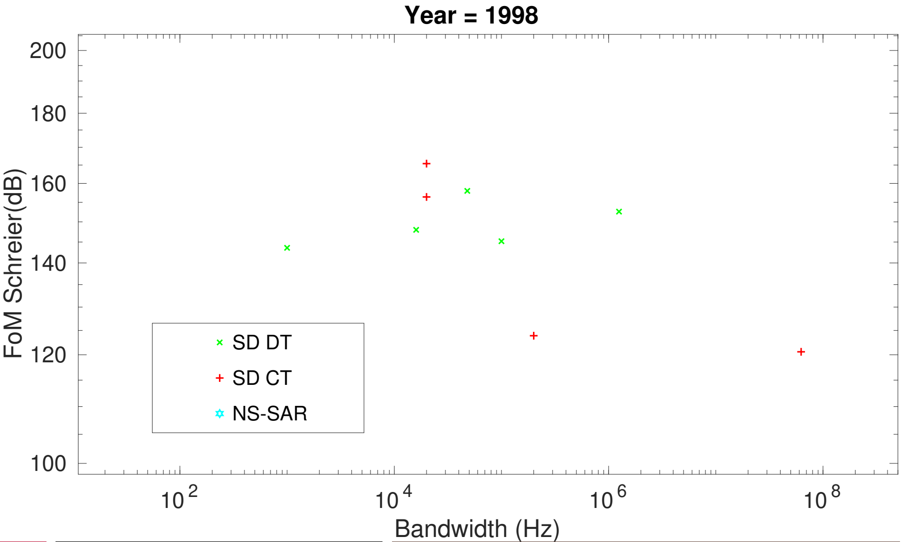

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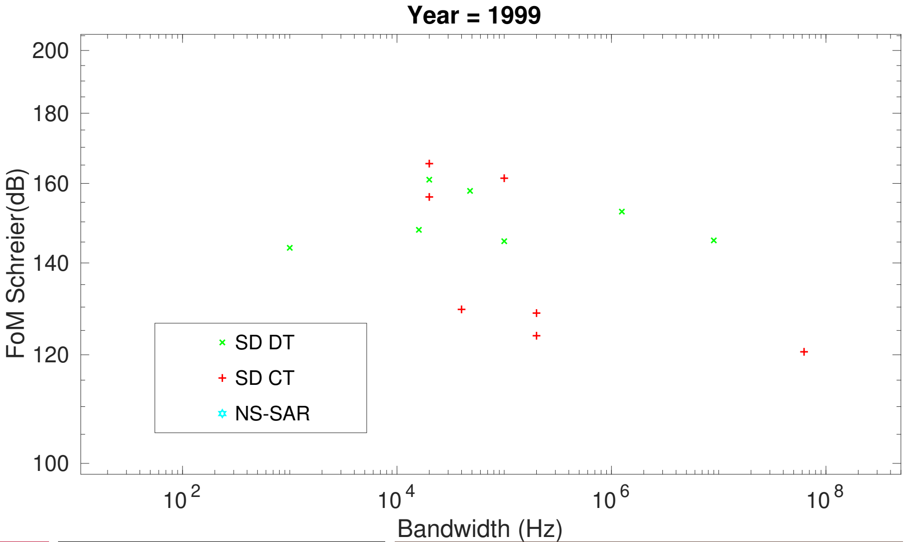
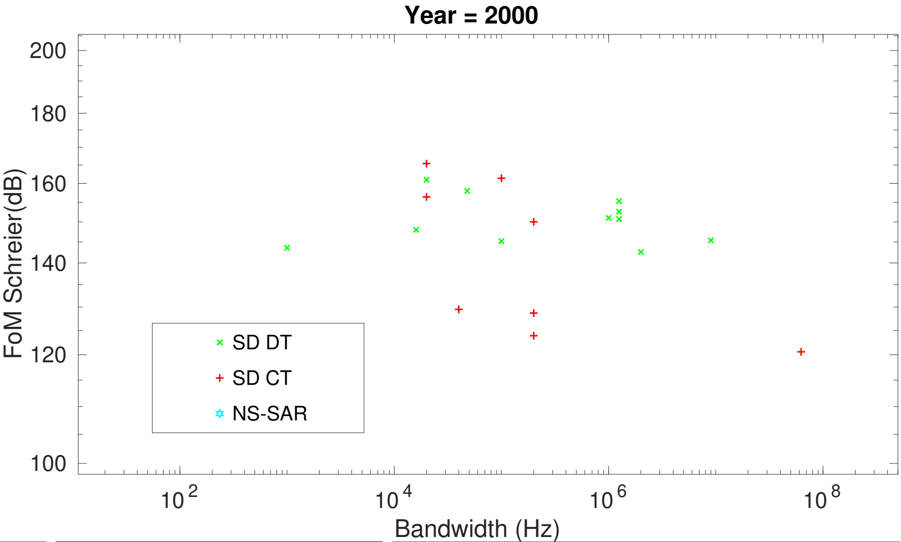


Evolution of the SOA



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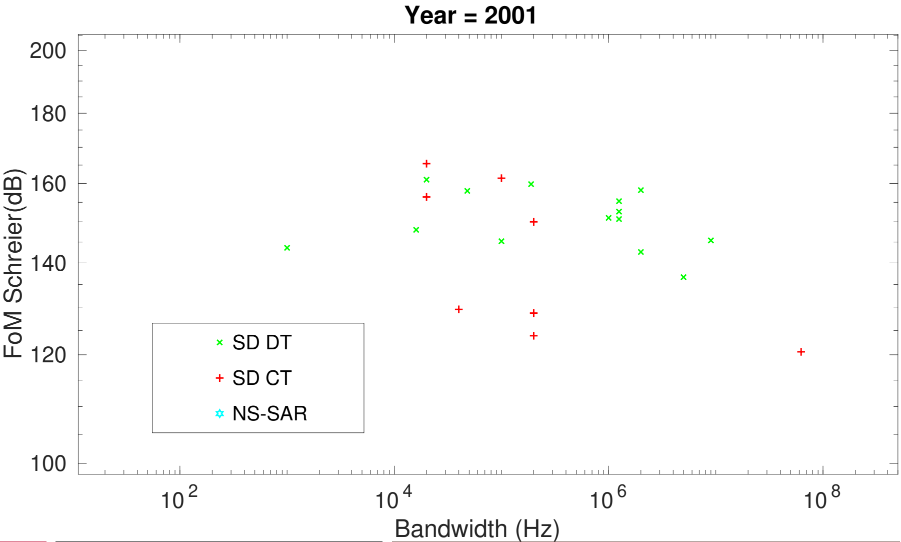

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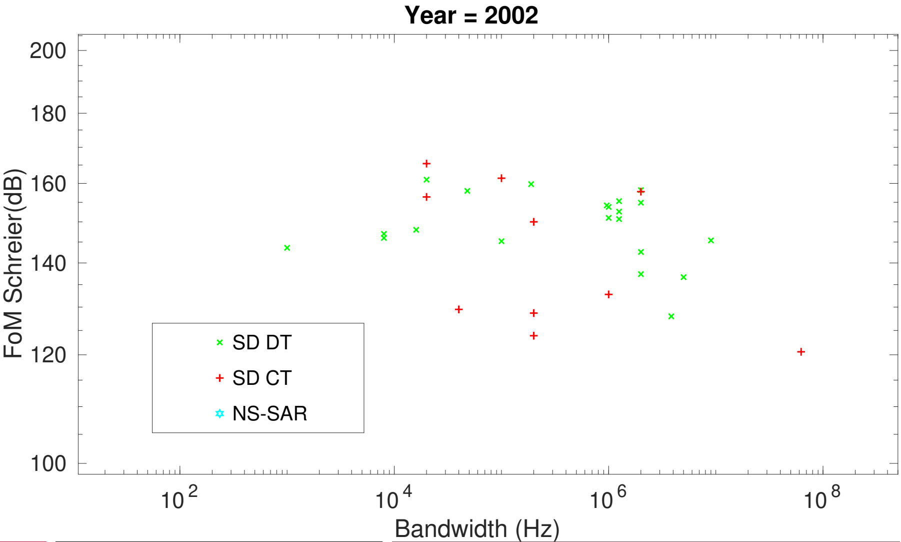

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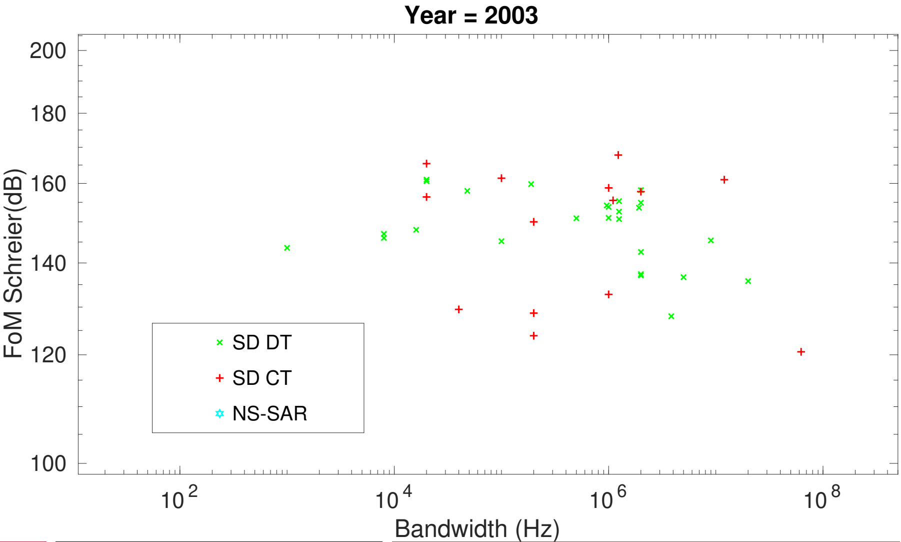

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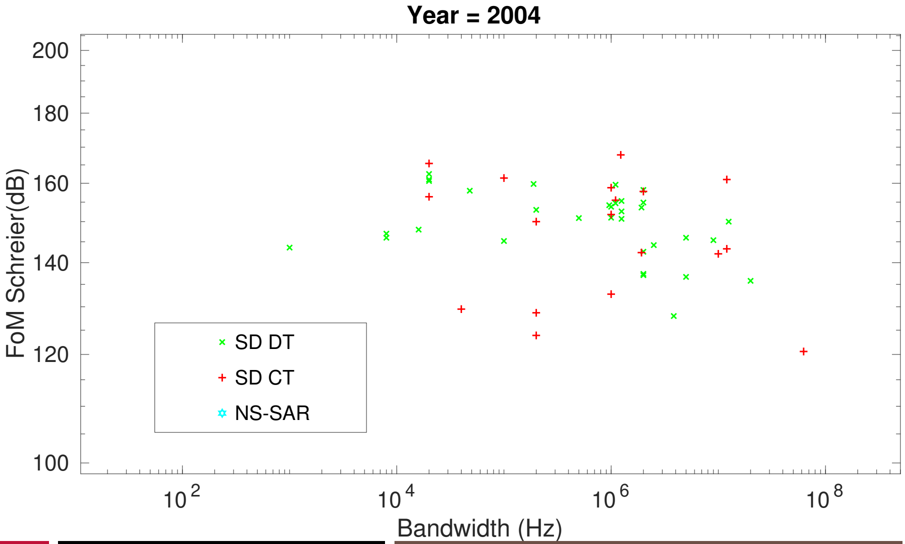

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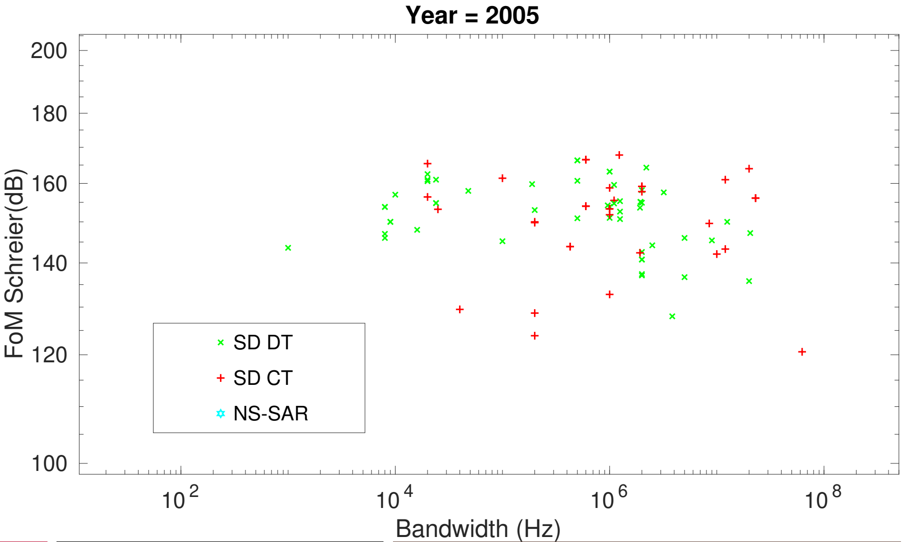

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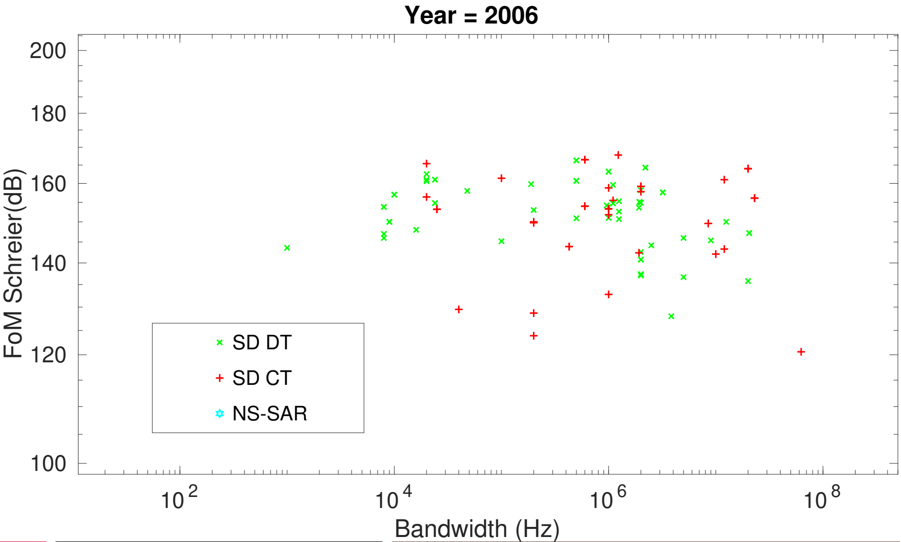

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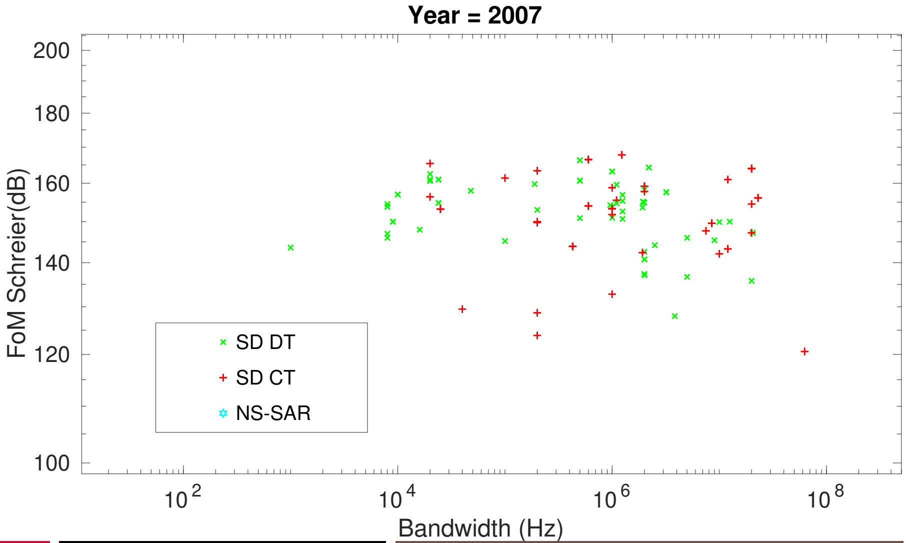

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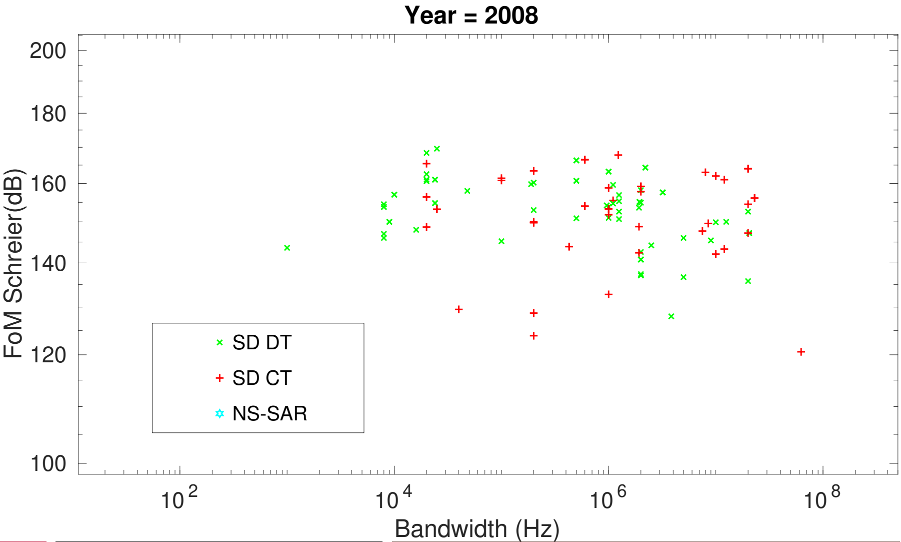

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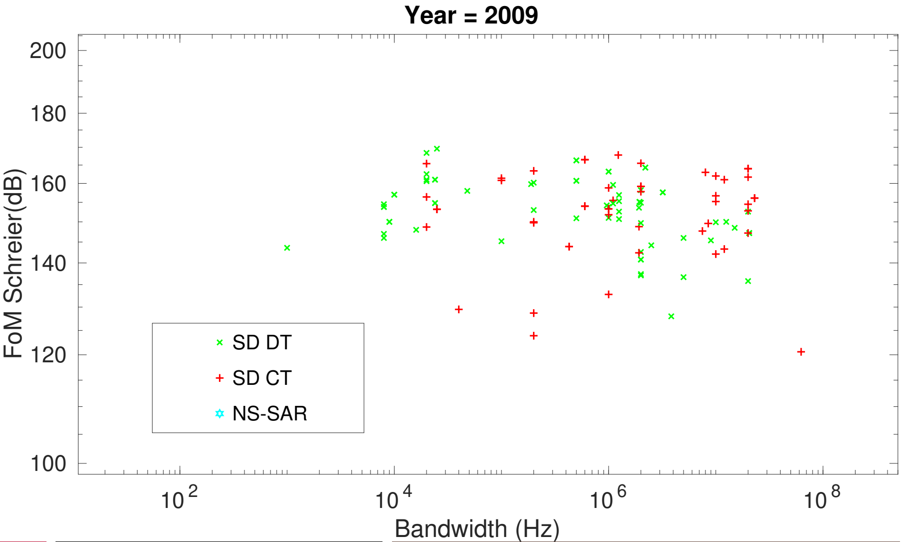

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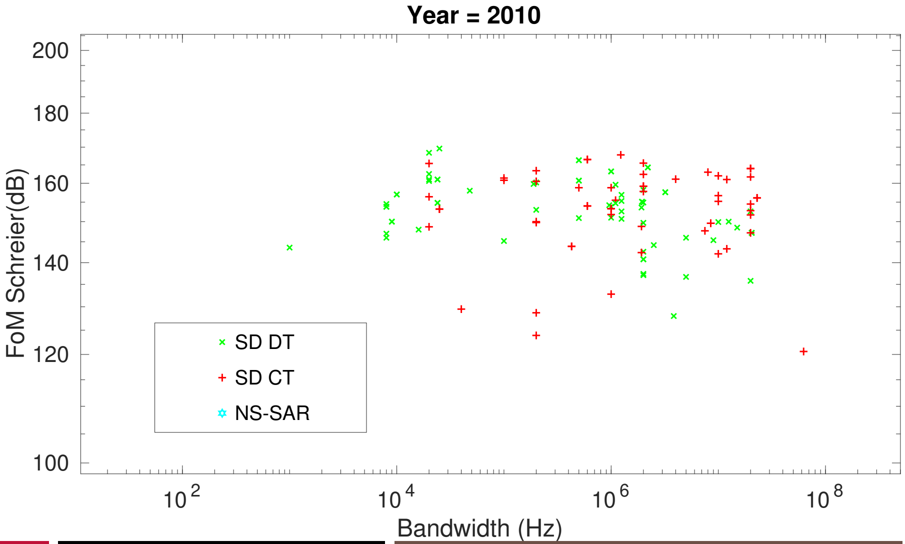

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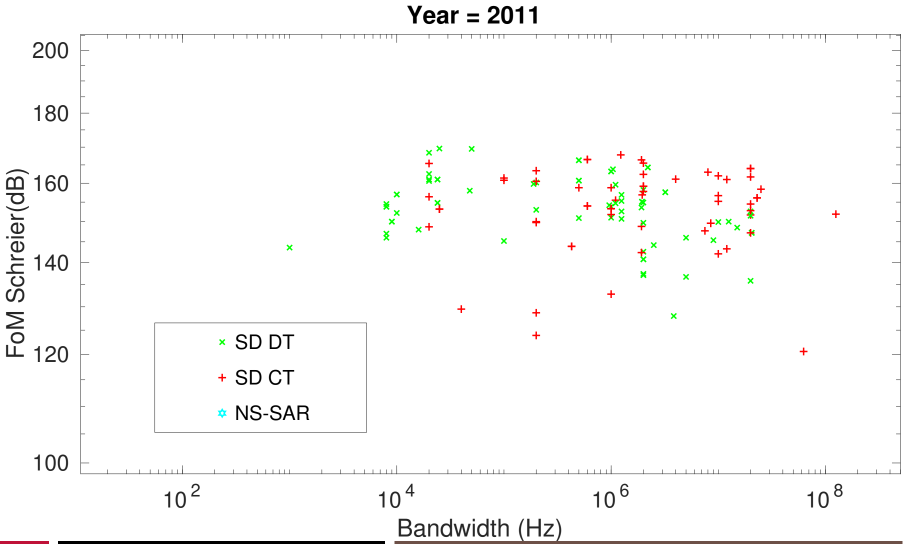

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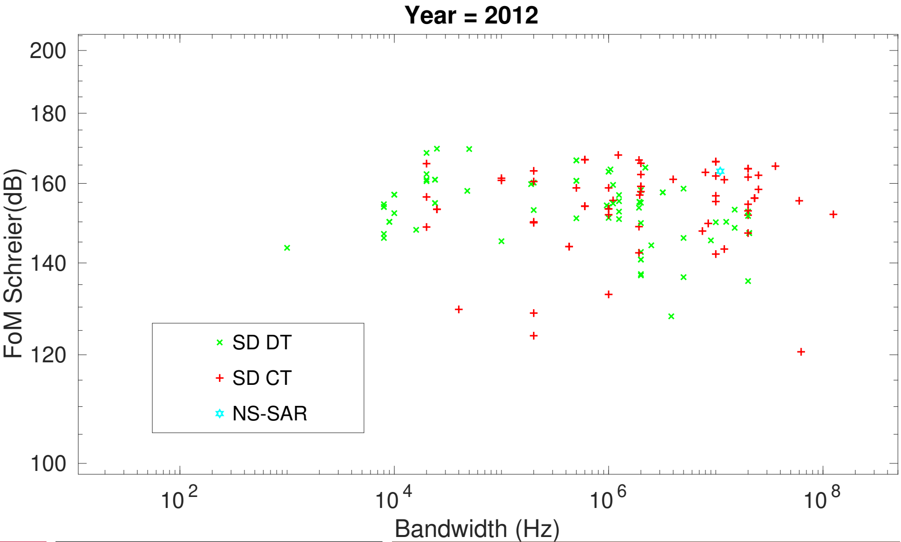
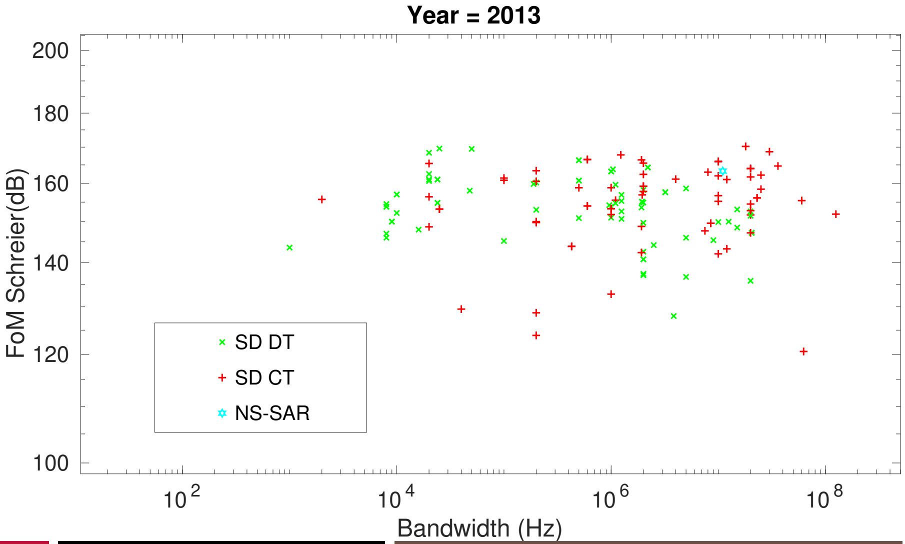


Evolution of the SOA



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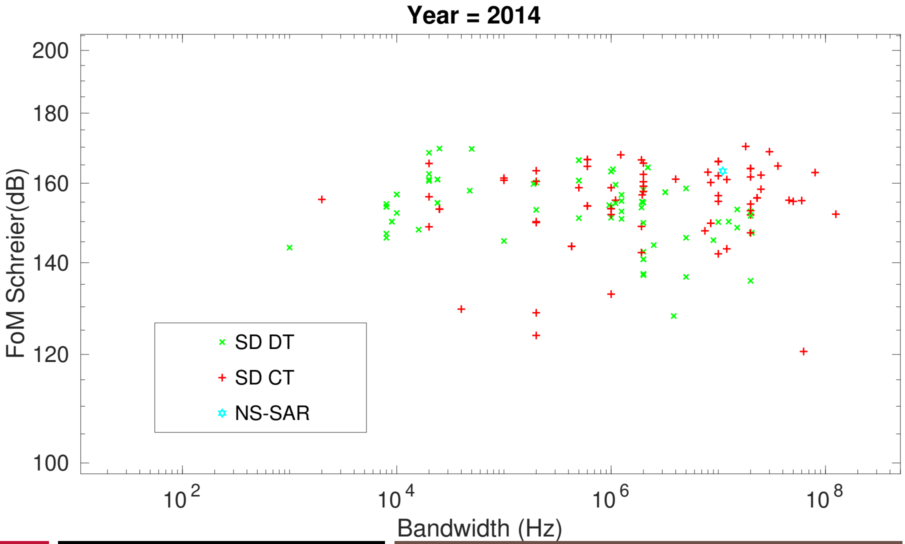

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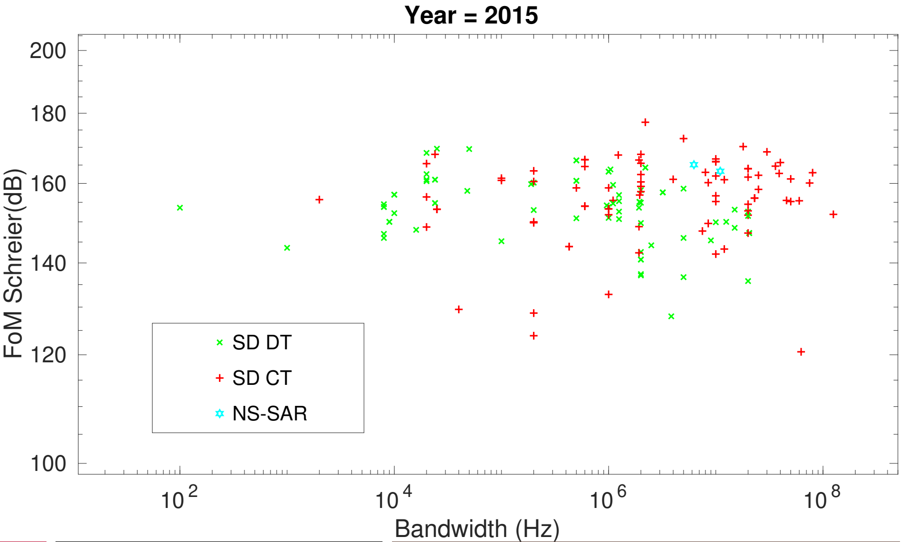

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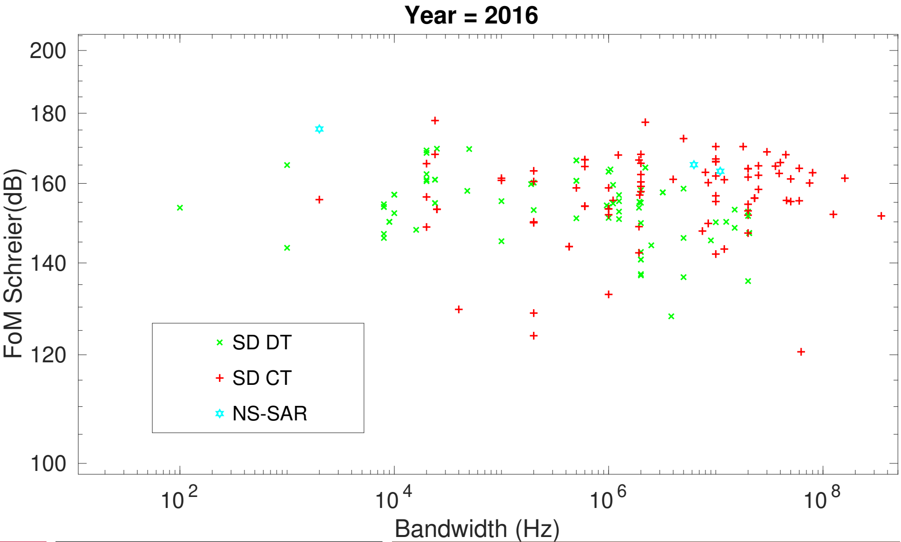

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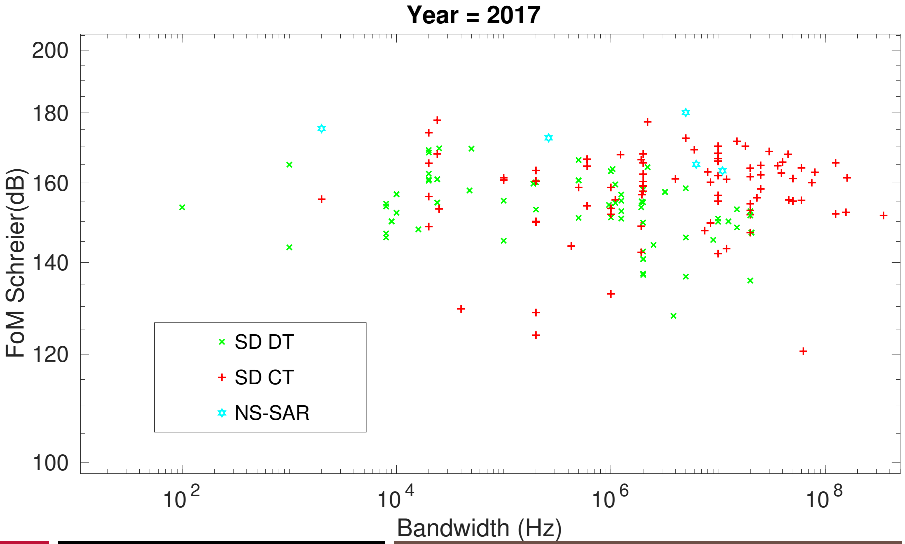

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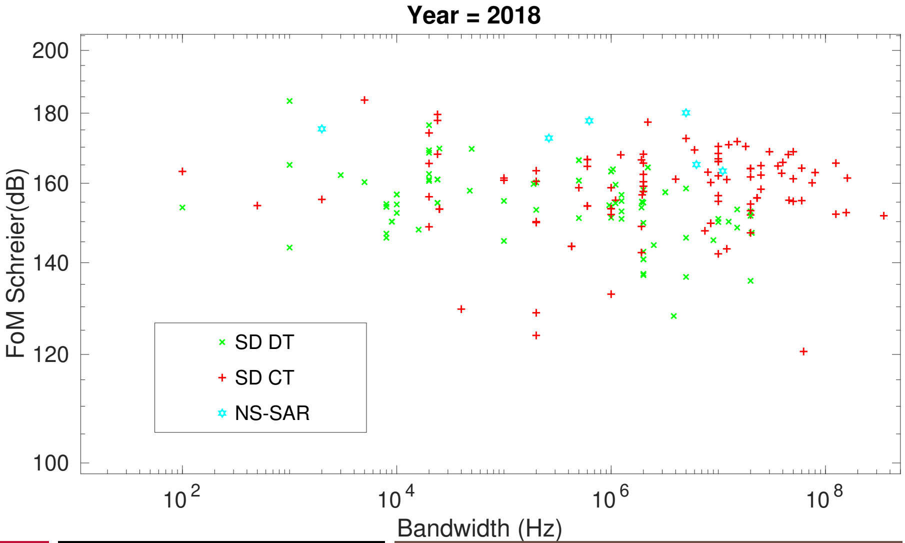

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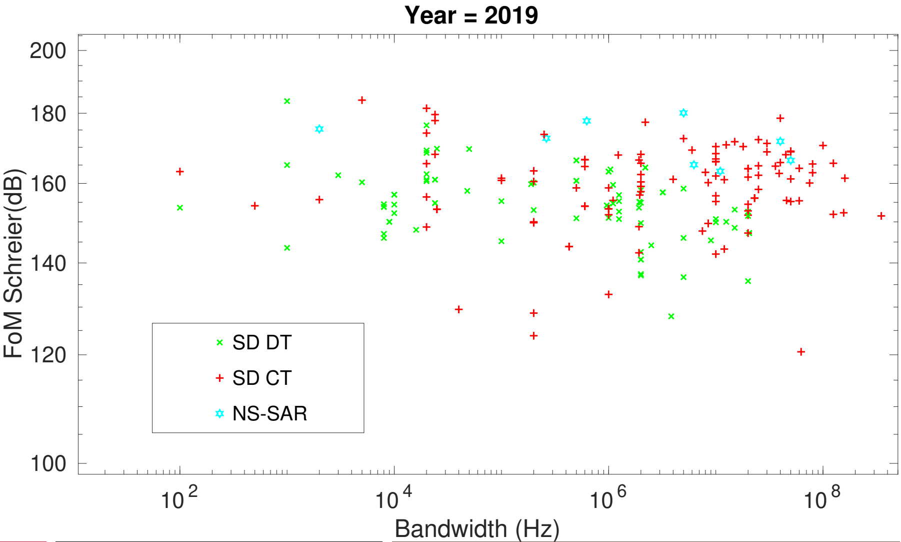

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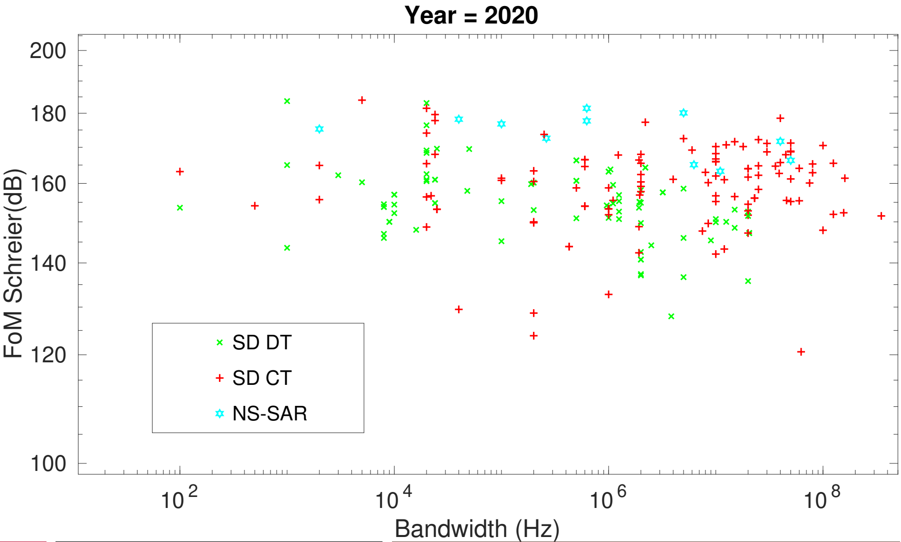

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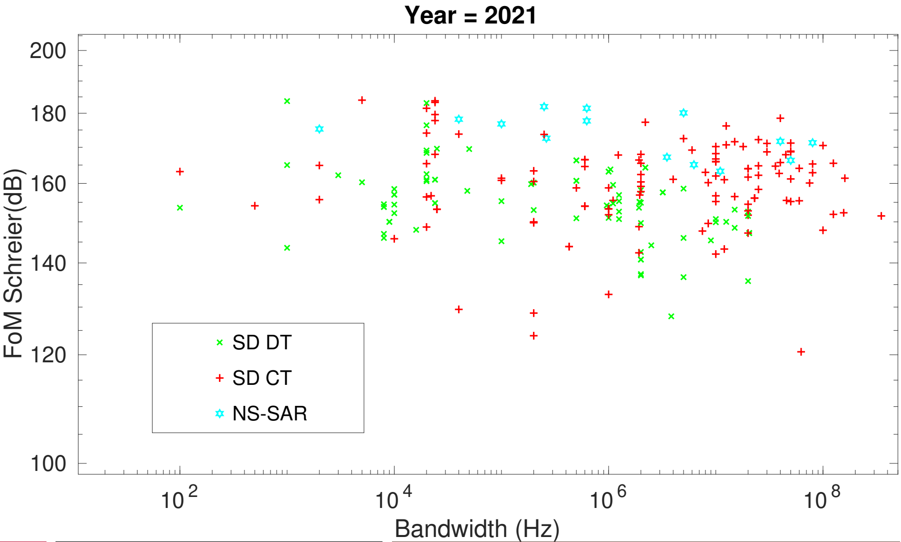

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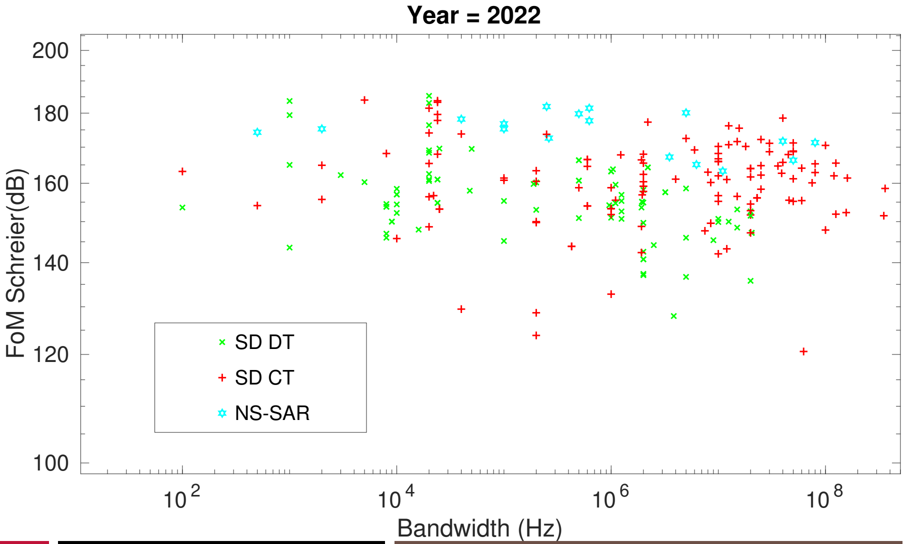

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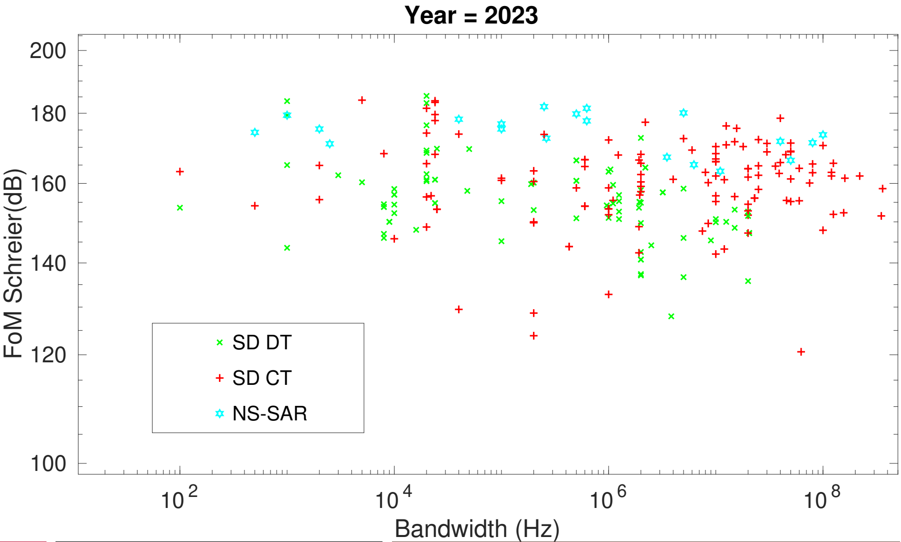

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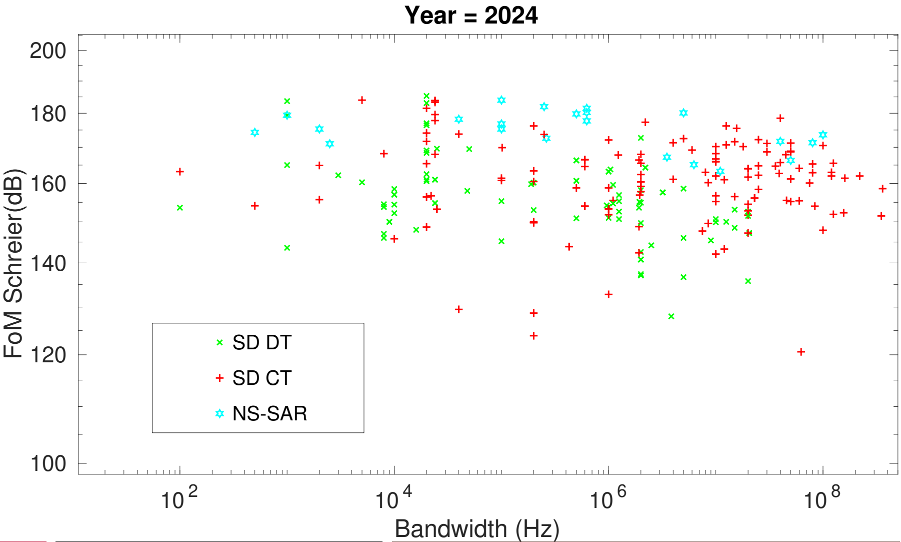
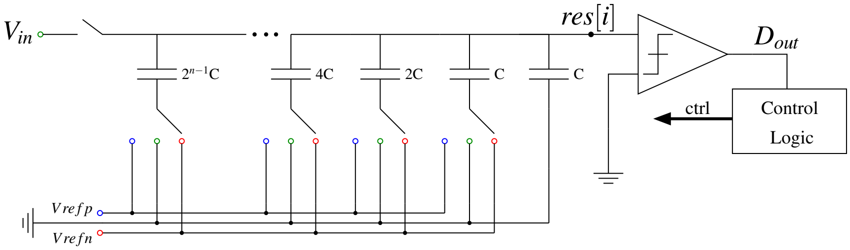
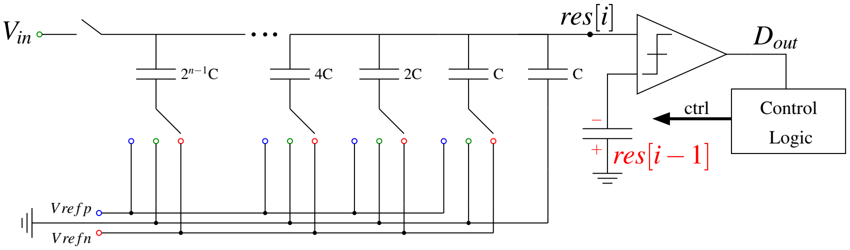


Noise Shaping SAR



Noise Shaping SAR

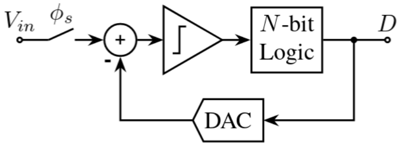


By linearizing the system, the quantization noise $N(z)$ is shaped as follows :

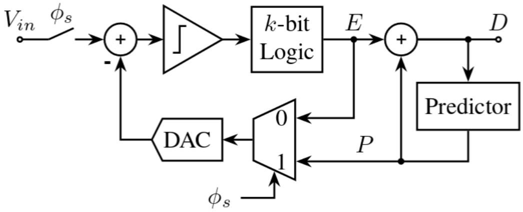
$$D_{out}(z) = Vin(z) + (1 - z^{-1})N(z)$$

The quantization noise is thus shaped to high frequencies improving the resolution in low frequencies

Prediciting SAR for gyroscope applications



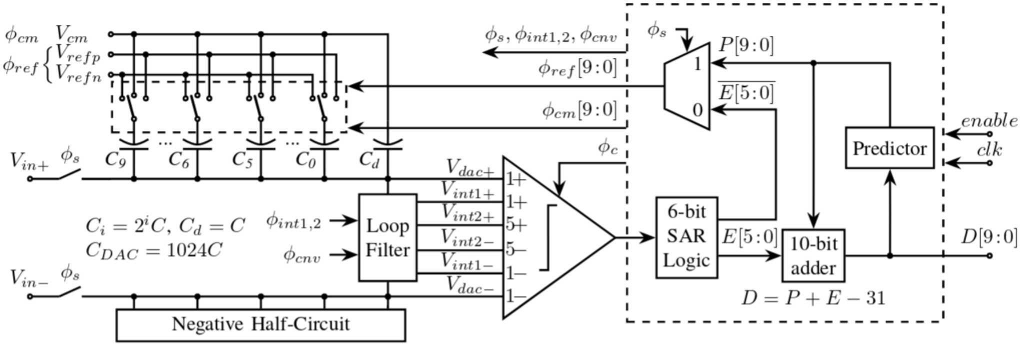
(a)



(b)

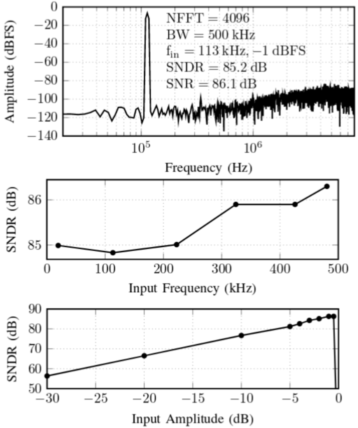
The idea is to profit from the knowledge of the characterisctics of the signal to predict the next sample range

Prediciting SAR for gyroscope applications



Implementation in 130 nm CMOS technology from TSMC

Comparison with SOA



Spec.	Zhua-19	Nam-22[1]	Lu-24[1]	This work
Tech. (nm)	40	90	55	**130**
Supply (V)	1.1	0.4	1	**1.2**
Sample rate (MS/s)	8.4	0.2	5	**16**
Oversampling ratio	16	10	32	**16**
Bandwidth (kHz)	262	10	6.25	**500**
Power (μW)	143	0.33	7.4	**270**
SNDR (dB)	78.4	58.5	91	**86.3**
ENOB (bit)	12.7	9.4	14.8	**14**
$\mathrm{FOM_W}$ (fJ/step)[2]	41	2.4	20.4	**16**
$\mathrm{FOM_S}$ (dB)[3]	171	163	180.3	**179**

[2] $\mathrm{FOM_W} = \mathrm{Power}/\left(2^{\mathrm{ENOB}} \times 2 \times \mathrm{BW}\right)$

[3] $\mathrm{FOM_S} = \mathrm{SNDR} + 10 \times \log_{10}\left(\mathrm{BW}/\mathrm{Power}\right)$

Outline

What are Delta Sigma Modulators ?

From Analog to Digital

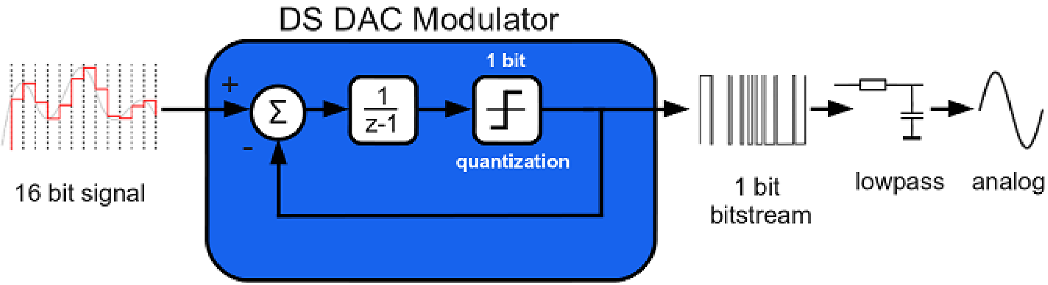
High speed Delta Sigma DACs

Spatio-temporal DSM in a massive MIMO system

Conclusion

Delta Sigma DAC

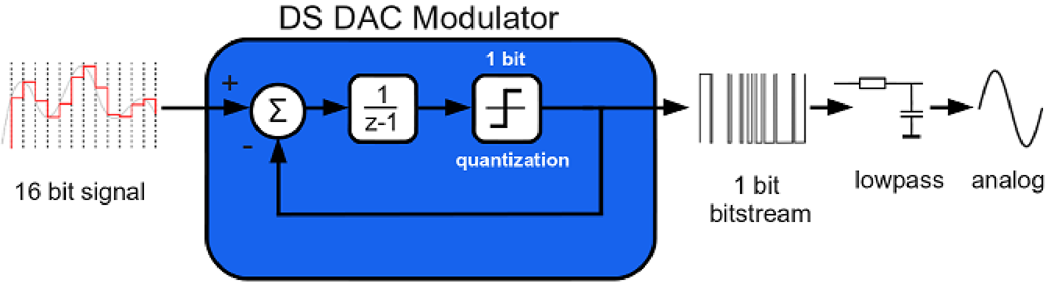
Delta Sigma modulation is used to compress the signal before the DAC



- Advantages : High resolution, low DAC complexity, high linearity
- Challenges : OOB noise, **low conversion bandwidth**

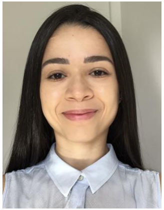
Delta Sigma DAC

Delta Sigma modulation is used to compress the signal before the DAC

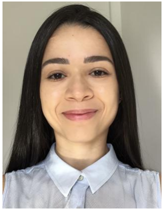


It is not possible to carry out simple time interleaving as the current output depends on the previous states

How to increase the Delta Sigma speed



How to increase the Delta Sigma speed



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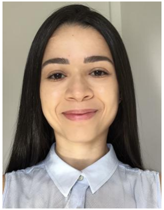
Multi-staging

How to increase the Delta Sigma speed



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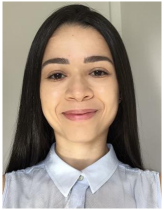
Multi-staging

How to increase the Delta Sigma speed



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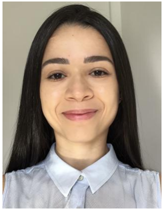
Multi-staging Unrolling

How to increase the Delta Sigma speed



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Multi-staging

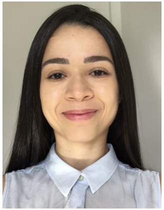
↓

Unrolling

↓

Zero Padding

How to increase the Delta Sigma speed



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Multi-staging

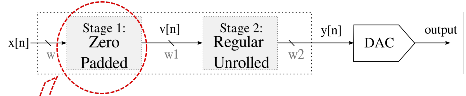
↓

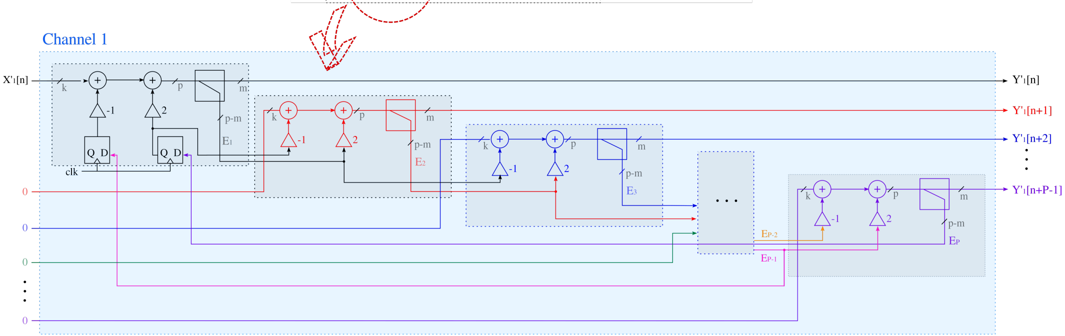
Unrolling

↓

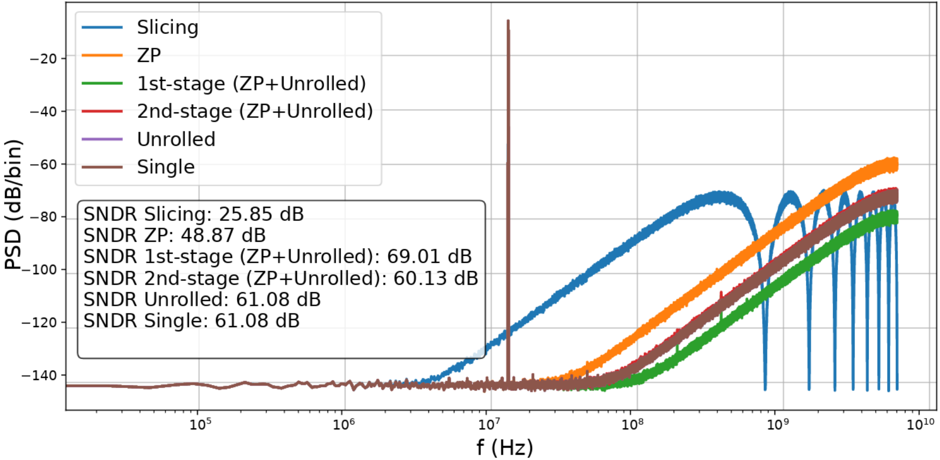
Zero Padding

Proposed architecture





Results



Order=2, OSR=10, Nbits=4

Synthesis Results in GF 22 nm

Unrolling factor	SNDR (dB)	Output levels	Throughput (GS/s)	Area (μm^2)	Power (mW)
ZP					
2	58.16	19	17.94	1022	18.71
4	55.17	23	33.24	2536	44.27
8	52.02	31	65.04	6618	114.17
16	48.87	35	108.96	20679	346.94
Unrolling + Unrolling					
16	61.08	17	57.92	4751	91.32
ZP + ZP					
16	48.51	35	136.48	21334	342.03
ZP + Unrolling					
2	60.98	17	20.70	1130	22.92
4	60.80	17	35.72	2471	43.06
8	60.58	17	56.32	4829	63.97
16	60.13	19	85.92	14431	218.24

Comparison with SOA

Ref.	SNDR (dB)	BW (MHz)	Order	Throughput (GS/s)	Technology /Platform	Architecture
Johanson-14	N/A	62.5	3	2	65nm	SPDSM
Podsiadlik-14	N/A	1.25	2	0.4	FPGA	Polyphase
Su-15	72	500	3	8	65nm	Unrolled
Marin-15	67	160	3	6	28nm FDSOI	Polyphase
Cordeiro-16	31	122	1	3.2	FPGA	Slicing
Su-18	70	600	3	12	65nm	Multi-stage
Wang-19	N/A	252	4	5	FPGA	Slicing
Park-24	30.7	268	2	4.3	65 nm	Unrolled
Laguna-24	72	0.05	2	0.012	FPGA	AnalogMux
Zhong-25	32	2316	4	25.78	FPGA	Slicing
This work	**60/74**	**4250/2125**	**2**	**85**	**22nm FDSOI**	**ZP+Unrolled**

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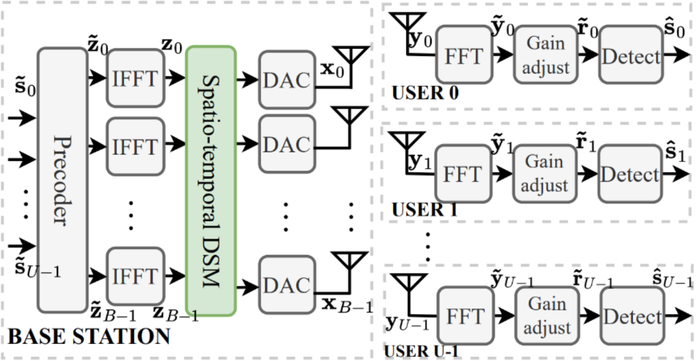
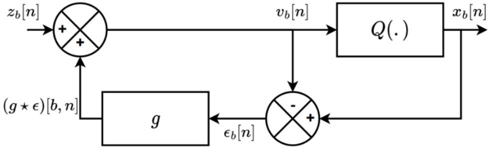
Context



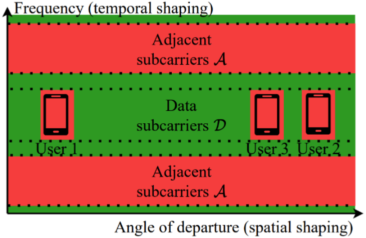
Reducing DAC resolution is one the major concerns for mMIMO systems.

Spatio-temporal DSM



$$(g \star \epsilon)_b[n] = \sum_{\ell=0}^{T_{\text{ant}}-1} \sum_{m=0}^{T_{\text{time}}-1} g_\ell[m]\epsilon_{b-\ell}[n-m]$$

Spatio-temporal DSM block diagram



Ideal NTF

$$X(f,\phi) = Z(f,\phi) + \underbrace{(1 + G(f,\phi))}_{\text{NTF}} E(f,\phi)$$

Spatio-temporal DSM consists in shaping noise both in frequencies and in angles

Problem Formulation

$$\min_{g,\mu,\zeta} \quad \mu + w\zeta$$

$$\text{s.t.} \quad \sqrt{\mathbb{E}[|\tilde{d}_u[k]|^2]} \leq \mu \quad \forall u \in \text{Users}, k \in \text{Data subcarriers}$$

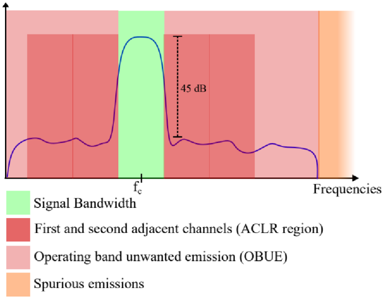
$$\text{g verifies a stability constraint}$$

$$\sqrt{\int_{f \in \mathcal{A}} ||1 + G(f,\phi)|^2} \leq \zeta \quad \forall \phi$$

Adjacent frequencies

ITF

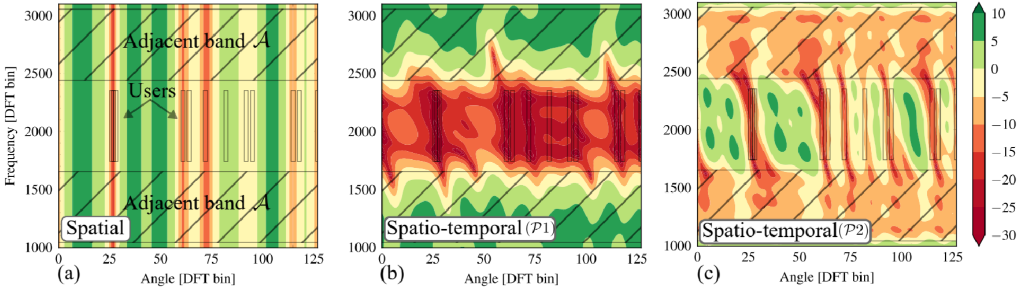
All directions of space



Adjacent Channel Leakage Ratio (ACLR) fixes the allowed leakage to the adjacent channel

Simulation Results

What we obtained



(a) Spatial : Noise Shaping only on angles
(b) P1 focuses just on Inband
(c) P2 is a tradeoff beteween ACLR and BER

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Conclusion

Delta Sigma is the solution for all the problems,

Conclusion

Delta Sigma is the solution for all the problems, it is actually a sect

You can check out any time you like, but you can never leave

Thank you

Thank you

Questions !

- **Viet Nguyen, Tien Nguyen and Nicolas Delorme** : Prediciting Noise Shaping SAR ADC
- **Evelyn Lima and Yves Mathieu** : High Speed multi-stage DSM ZP-Unrolled DAC
- **Nicolas Schlegel and Philippe Ciblat** : Spatio-temporal DSM in a massive MIMO system

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Design methodologies

The most popular tool to design Delta Sigma modulators is the “Schreier DS Toolbox“ :

Example of workflow :

OSR=20 ; order = 3 ; Hinf= 6 ; nbits=3

1-Specify the specifications of the needed modulator : OSR, order, outof-band Gain, nbits
2-Using function `synthesizeNTF`, we can generate the NTF expression
3-Using function `simulateDSM`, we can make a transient simulation
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The toolbox contains around 100 functions

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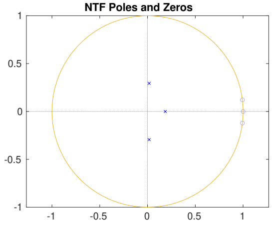
```
H =

        (z-1) (z^2 - 1.985z + 1)
  ------------------------------------
  (z-0.1855) (z^2 - 0.03384z + 0.08669)
```



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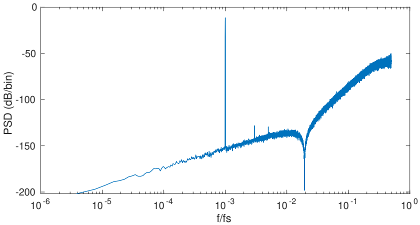

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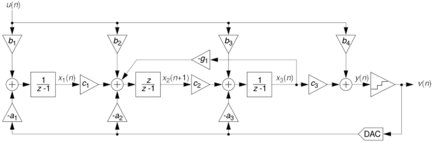
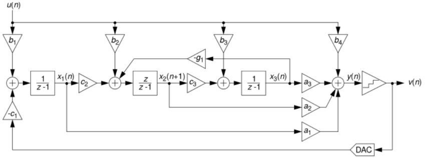
Cascade of Resonators in FeedBack (CRFB)



Odd Order

Cascade of Integrators in FeedForward (CIFF)



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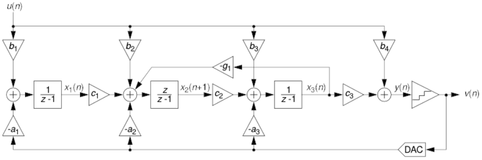
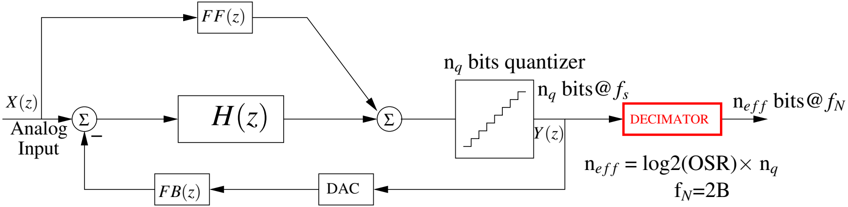
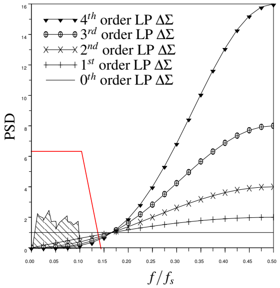
```
>> [a,g,b,c] = realizeNTF(H,'CRFB')
a =
    0.8575    1.7819    0.9839
g =
    0.0148
b =
    0.8575    1.7819    0.9839    1.0000
c =
     1     1     1
```



Odd Order

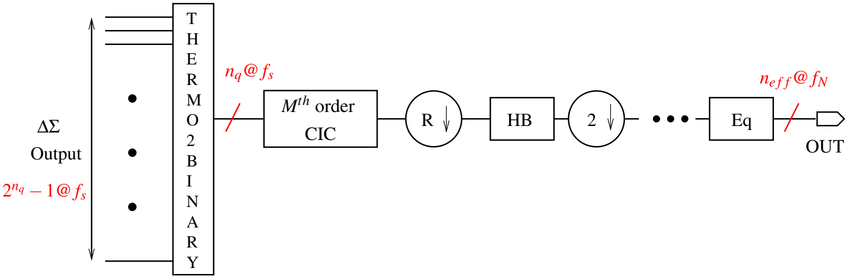
Decimator





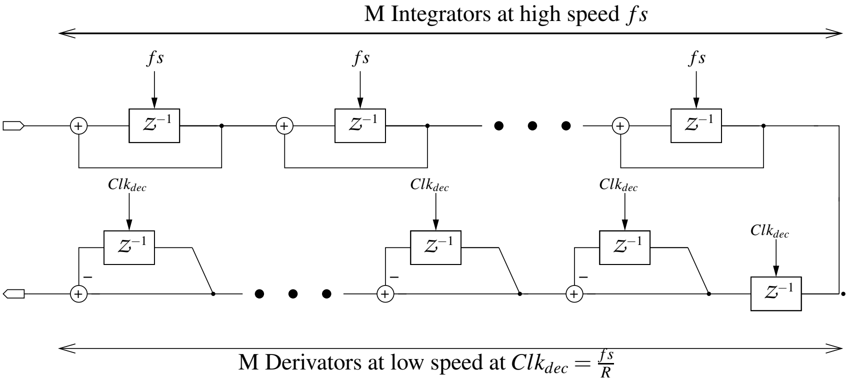
$NTF(z) = (1 - z^{-1})^P$

Classical architecture



- Cascaded comb filter (CIC) : very simple to implement but inband drop
- Half Band Filters : half complexity
- Equalizer at Nyquist Rate to correct the CIC drop

Classical architecture



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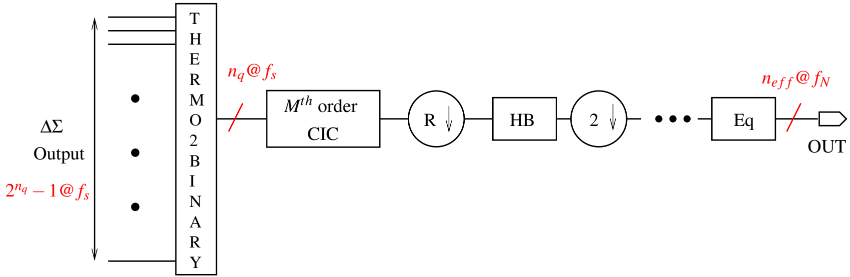

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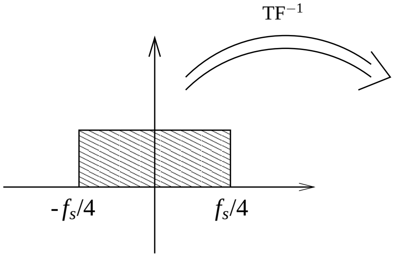

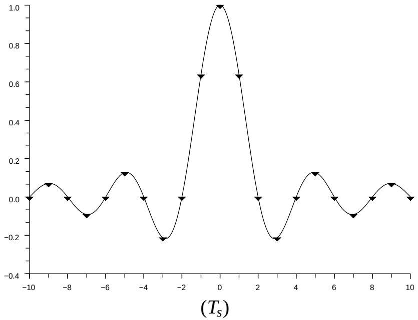

$\alpha sinc(\frac{f_s.t}{4})$

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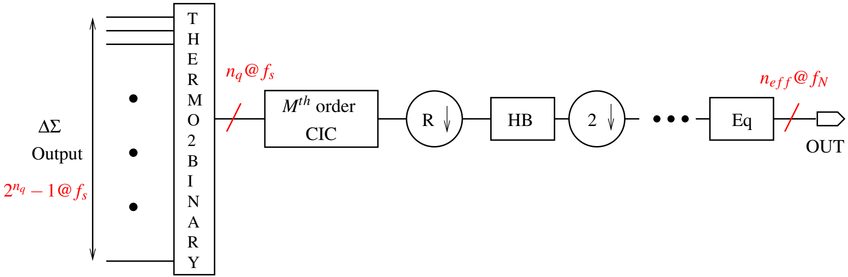

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What's next for NS SAR and $\Delta\Sigma$ ADCs

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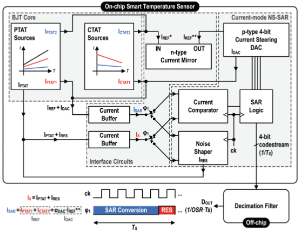

Arpile et al 2024

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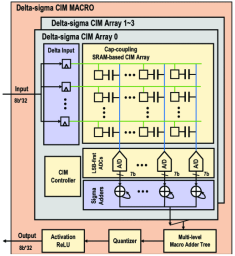
- More co-integration between the ADC/sensors
- Compute in Memory ADC

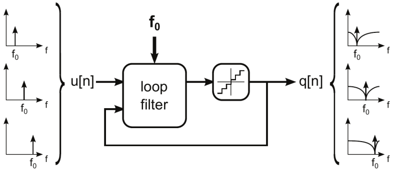


Chen et al 2023

Receivers

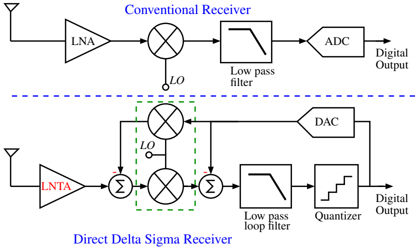
Delta Sigma based systems where the input is RF and the output is digital

Bandpass Delta Sigma



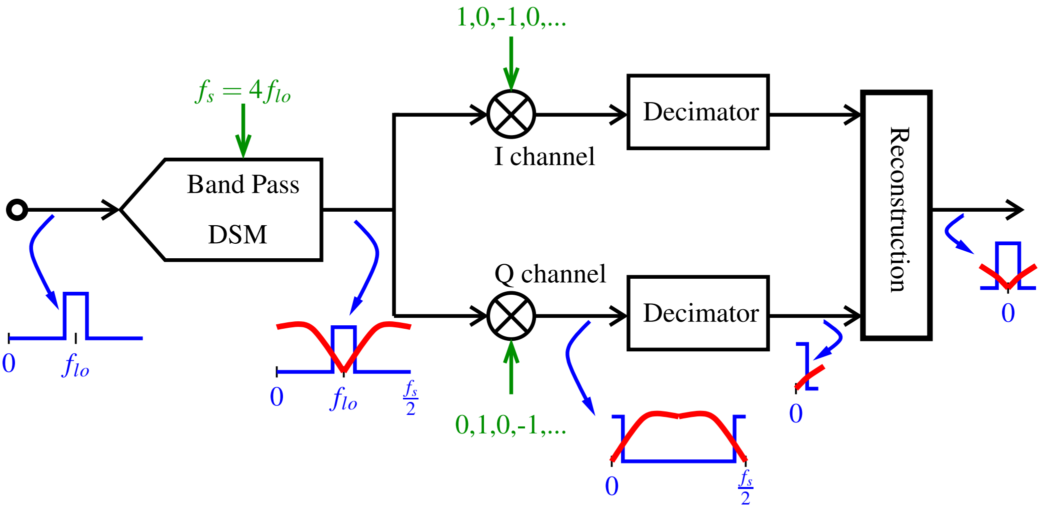
- Bandpass modulator
- The down-mixing is done in digital

Direct Delta Sigma Receiver



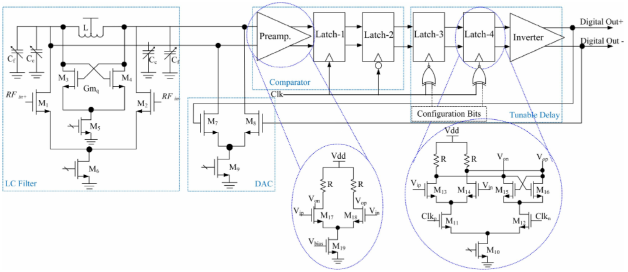
- Integrates the RF blocs in DSM loop
- The output is directly in baseband

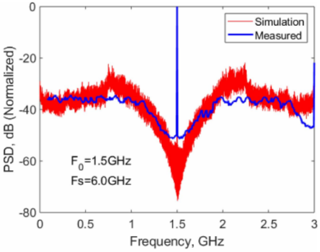
Bandpass Delta Sigma



Implementation

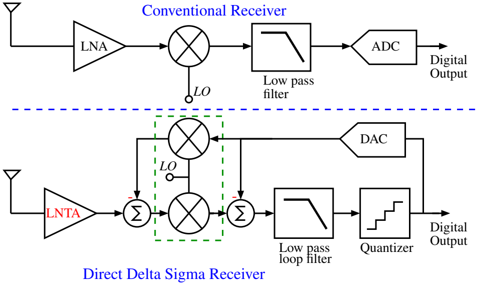
[Sayed et al 2020]





The implementation is often done using LC filter with $f_{LO} = f_s/4$

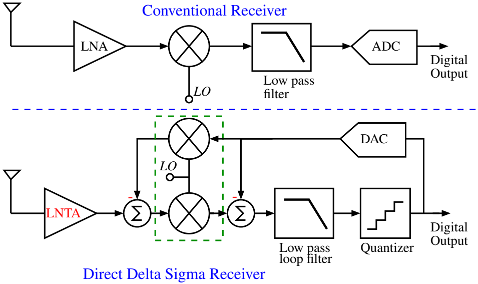
DDSR vs conventional receiver



Main advantages of the RF feedback

- Relaxing the linearity requirements as the signal swing is reduced
- Increasing the Noise Transfer Function order

DDSR vs conventional receiver



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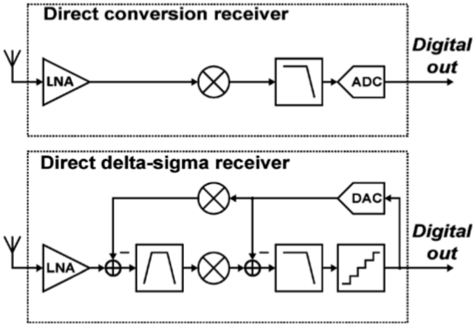
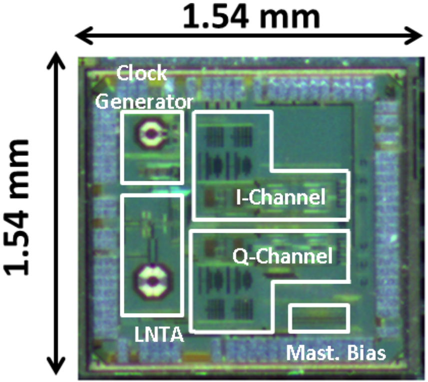
Main challenges in the architecture

- The conventional design approaches can not be applied directly to the DDSR
- Noise coupling due to the RF DACs

DDSR vs conventional receiver





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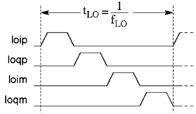
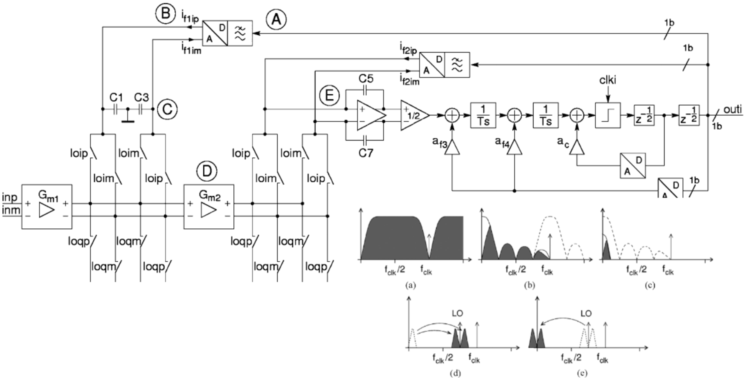
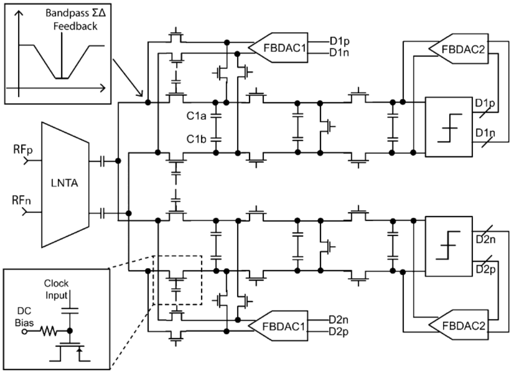




[Koli et al 2010]

Fully active CT Implementation with independent f_{LO} and f_s

Implementation



[Wu et al 2014]

Passive DT Implementation with $f_{LO} = f_s$

Conclusion and challenges on DSM based receivers

- The architecture design is challenging and requires good knowledge in both ΔΣ and RF blocks (LNA and mixers)
- The RF feedback degrades the noise performance of the architecture at the cost of a better linearity
- The ratio between the RF coefficient and the LNA gain allows to play on the noise/linearity/sensitivity tradeoff
- Bandpass DSM has the advantages of being robust against I/Q mismatch but requires higher clock (4 flo)
- De-correlating the filtering (STF) from the quantization noise performance (NTF) is another aspect to investigate